TAMAGAWA SEIKI CO.,LTD.

Smartcoder®

AU6805

USERS MANUAL

MNL000634W00-0200

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Safety Precautions

Caution !	Before use Smartcoder, please carefully read the specification and this manual for proper use. Incorrect usage do not operate normally, may damage the equipment that is connected to this product or this product. Retain this manual, and please re-read when in doubt.

■Notes

Smartcoder (AU6805) is an integrated circuit (i.e electronic device) with a high grade quality level, but the predictable failure rate is not zero. Also there are some possibility to do unplanned work cause of noise, static electricity, wiring error, etc. The user is advised, therefore, that multiple safety means be incorporated in your system or product so as to prevent any consequential troubles resulting from the failure of our smartcoder (AU6805).

These application samples which listed in this manual are reference examples. If you use these examples, please make sure that you understand your system, equipments, and those functions and safety.

And the content written in this manual might be changed as needed. For the latest content, please contact your sales representative.

■Product Warranty

(1)Warranty Period

The warranty period for Smartcoder (AU6805) is one year after shipping. Failed products within this warranty period will be replaced with new one.

(2)Coverage

Even if within the warranty period, we will not take responsibility for the products which show quality degradation caused by deviant usage against this document or specification like below.

- ・In case of usage of unguaranteed condition/environment/handling nonlisted in this manual or specification.
- ・In case of Remodeling/Repair which is not done by Tamagawa-seiki.
- ・In case of misusing this product.
- ・In case of unforeseen matters which can not expect at technology level of shipping age

1. Introduction

1.1 Product Overview

Smartcoder(AU6805)is an R/D (Resolver to Digital) conversion IC used with a brushless Resolver (BRX) such as Singlsyn, Smartsyn, etc. It converts the electrical information (analog signal) corresponding to a mechanical rotational angle of the Resolver to the corresponding digital data and output it.

This IC applies a proven R/D conversion method "Digital Tracking Method", and be possible to provide a low- cost and many kind of angle detection applications while ensuring high reliability of resolver(syncro) system.

1.2 Product Features

■Real time output

Max tracking rate : 240,000min^{-1}(Loop gain: fixed value setting)

Max angular acceleration : 1,000,000rad/s^{2}(Loop gain: Auto tuning)

■All-in-one design

Eliminates phase adjustment of exciting signal (allowable phase angle :±45° while exciting signal 1 period is 360°).

Implemented an Oscillator and excitation amplifier (current control type) help to reduce system cost.

■Small・Light weight

7×7mm(Pin pitch: 0.5mm、48pin-LQFP、weight: 0.2g)

■Enhance error detection function

Followings are implemented. Abnormal Resolver Signal; Breaking of Resolver Signal Line; Abnormal R/D conversion; Abnormal High temperature inside IC.

■Implemented BIST(Built-In Self Test)function

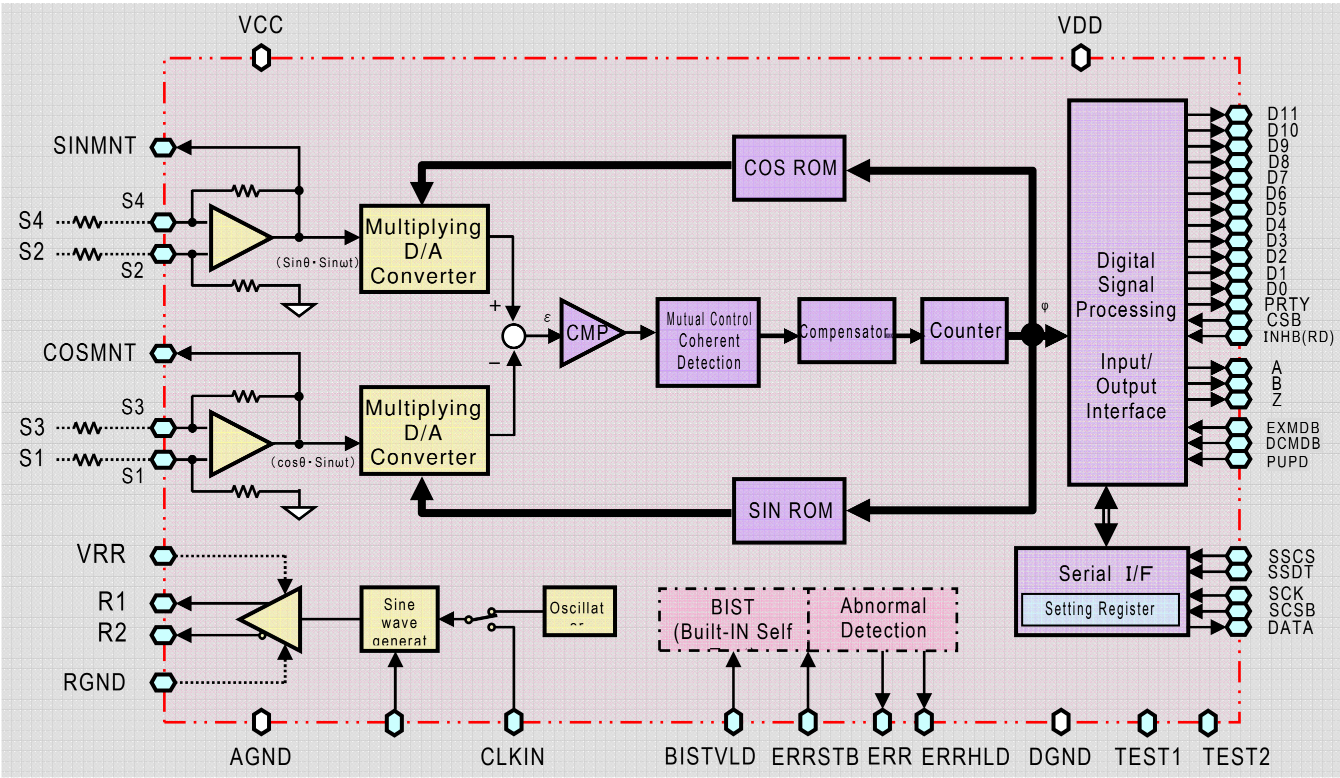
R/D conversion function and breaking detection of signal line can be tested by themselves.

■Rich output form

Binary-code Parallel 12bit Bus compatible、Positive logic＋ A,B,Z ＋ Serial I/F

■DC+5V Single Power Supply

1.3 Block Diagram



1.4 Spec Overview

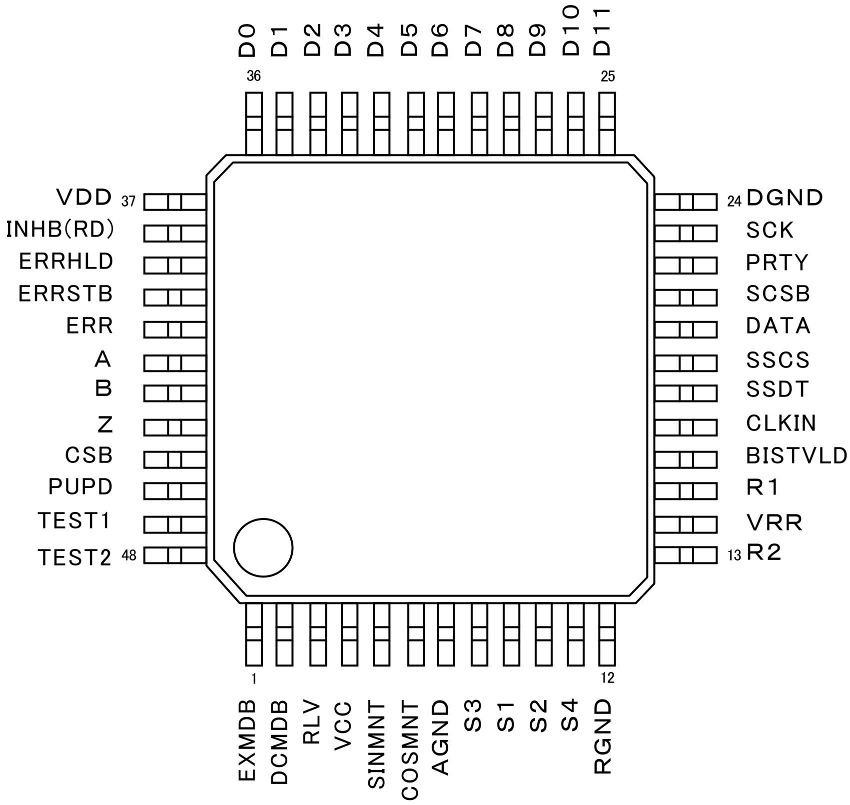
Output form	Binary code parallel 12bit bus compatible, Positive logic ＋ A, B, Z ＋ Serial I/F
Resolution	4,096 (2^{12})
Conversion accuracy (Static)	±4 LSB
Settling time (Step input 180° in electric angle)	42 ms typ. (Loop Gain Fixed Value setting① (Bandwidth 800Hz)) 17 ms typ. (Loop Gain Fixed Value setting② (Bandwidth 2,000Hz)) 14 ms typ. (Loop Gain Fixed Value setting③ (Bandwidth 2,500Hz)) 24 ms typ. (Loop Gain Fixed Value setting④ (Bandwidth 1,500Hz)) 35 ms typ. (Loop Gain Fixed Value setting⑤ (Bandwidth 1,000Hz)) 69 ms typ. (Loop Gain Fixed Value setting⑥ (Bandwidth 500Hz)) 170 ms typ. (Loop Gain Fixed Value setting⑦ (Bandwidth 200Hz)) 1.5 ms typ. (Loop Gain Auto-tuning setting)
Max. tracking rate	240,000 min^{-1} (Loop Gain Fixed Value setting) 120,000 min^{-1} (Loop Gain Auto-tuning setting) 15,000 min^{-1} (Loop Gain Fixed Value setting、Serial Absolute Output 16BIT setting) 12,000 min^{-1} (Loop Gain Auto-tuning setting、Serial Absolute Output 16BIT setting)
Max. angular acceleration	230,000 rad／s^2 typ. (Loop Gain Fixed Value setting① (Bandwidth 800Hz)) 1,110,000 rad／s^2 typ. (Loop Gain Fixed Value setting② (Bandwidth 2,000Hz)) 1,370,000 rad／s^2 typ. (Loop Gain Fixed Value setting③ (Bandwidth 2,500Hz)) 800,000 rad／s^2 typ. (Loop Gain Fixed Value setting④ (Bandwidth 1,500Hz)) 290,000 rad／s^2 typ. (Loop Gain Fixed Value setting⑤ (Bandwidth 1,000Hz)) 70,000 rad／s^2 typ. (Loop Gain Fixed Value setting⑥ (Bandwidth 500Hz)) 7,000 rad／s^2 typ. (Loop Gain Fixed Value setting⑦ (Bandwidth 200Hz)) 3,000,000 rad／s^2 typ. (Loop Gain Auto-tuning setting)
Response (As output response delay in electric angle)	±0.2° Max./10,000 min^{-1}
Encorder emulation output(A,B)	1,024 C/T
Resolver excitation amplifier (current control type)	10mArms、10kHz typ. (RLV=H) 20mArms、10kHz typ. (RLV=L)
Fault detection function	･Abnormal resolver signal ･Breaking of resolver signal line ･Abnormal R/D conversion ･Abnormal high temperature inside IC
BIST function (BIST: Built-In Self Test)	･BIST of R/D conversion (Test for R/D conversion) ･BIST of signal failure (Test for signal failure)
Power source	DC 5V±10% 45mA max. (RLV=H) DC 5V±10% 65mA max. (RLV=L)
Operating temperature	-40 ～ +125℃ (Do not exceed the Max. power consumption)
Storage temperature	-65 ～ +150℃ (before implementation)
Package Thermal Resistance ($R_{\theta JA}$)	63.6° /W (4-layer board: 76.2×114.3×t1.6)
Humidity	90% RH max. (No condensation)
Mass	0.2g typ.

1.5 Related Documents

（1） SPC009574W00　Smartcoder（AU6805） Specificaion

2. Pin List (Name and Functions)

2.1 Pin Assignment



2.2 Pin Description

<table>
<tr><th>Pin No</th><th>Symbol</th><th>Class</th><th>Description</th><th>Remarks chapter</th></tr>
<tr><td>1</td><td>EXMDB</td><td>D／I</td><td>Input/Output mode selection pin for R1,R2 (Pin13/Pin15).<table><tr><th>R1,R2 I/O mode</th><th>Exciting current output</th><th>Exciting signal input</th></tr><tr><td>EXMDB</td><td>H or Open</td><td>L</td></tr></table></td><td>(4.3.1(3))</td></tr>
<tr><td>2</td><td>DCMDB</td><td>D／I</td><td>Sensor selection pin.<table><tr><th>Sensor</th><th>Resolver</th><th>DC Resolver(ex: Hall IC)</th></tr><tr><td>DCMDB</td><td>H or Open</td><td>L</td></tr></table></td><td>(4.3.1(3))</td></tr>
<tr><td>3</td><td>RLV</td><td>D／I</td><td>Current selection pin when Pin1(EXMDB) set as exciting current output mode.<table><tr><th>Exciting current</th><th>10mArms.</th><th>20mArms.</th></tr><tr><td>RLV</td><td>H or Open</td><td>L</td></tr></table></td><td>(4.3.1(3))</td></tr>
<tr><td>4</td><td>VCC</td><td>――</td><td>Analog power pin. Connect to +5V.</td><td>(4.4)</td></tr>
<tr><td>5</td><td>SINMNT</td><td>A／O</td><td>Resolver signal (SIN) monitor output. Input gain should be adjusted by interface circuit to be approximately 2.5Vp-p for this pin.</td><td rowspan="2">(4.2.2)</td></tr>
<tr><td>6</td><td>COSMNT</td><td>A／O</td><td>Resolver signal (COS) monitor output. Input gain should be adjusted by interface circuit to be approximately 2.5Vp-p for this pin.</td></tr>
<tr><td>7</td><td>AGND</td><td>――</td><td>Analog ground pin. Connect to 0V.</td><td>(4.4)</td></tr>
<tr><td>8</td><td>S3</td><td>A／I</td><td>Resolver signal(S3) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.</td><td rowspan="4">(4.2.2)</td></tr>
<tr><td>9</td><td>S1</td><td>A／I</td><td>Resolver signal(S1) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.</td></tr>
<tr><td>10</td><td>S2</td><td>A／I</td><td>Resolver signal(S2) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.</td></tr>
<tr><td>11</td><td>S4</td><td>A／I</td><td>Resolver signal(S4) input pin. This signal enters through the gain setting resistor of resolver signal input circuit.</td></tr>
<tr><td>12</td><td>RGND</td><td>――</td><td>Exciting amplifier ground pin.. Connect to 0V.</td><td>(4.4)</td></tr>
<tr><td>13</td><td>R2</td><td>A／O(I)</td><td>Exciting signal(R2) I/O pin. Pin1(EXMDB) define I/O status. If set to output, sine-wave exciting current which can excite resolver directly generates between R1-R2 terminals. If set to input, input signal will be the resolver excitation signal that has been generated by an external oscillator, etc..</td><td>(4.2.1)
(4.2.3)</td></tr>
<tr><td>14</td><td>VRR</td><td>――</td><td>Exciting amplifier power pin.. Connect to +5V.</td><td>(4.4)</td></tr>
<tr><td>15</td><td>R1</td><td>A／O(I)</td><td>Exciting signal(R1) I/O pin. Pin1(EXMDB) define I/O status. If set to output, sine-wave exciting current which can excite resolver directly generates between R1-R2 terminals. If set to input, input signal will be the resolver excitation signal that has been generated by an external oscillator, etc..</td><td>(4.2.1)
(4.2.3)</td></tr>
<tr><td>16</td><td>BISTVLD</td><td>D／I</td><td>BIST function control pin.
BIST function can run when BISTVLD pin set L level and serial setting register set for BIST operation code.<table><tr><th>BIST control</th><th>Not execution</th><th>Executable</th></tr><tr><td>BISTVLD</td><td>H or Open</td><td>L</td></tr></table></td><td>(7)</td></tr>
<tr><td>17</td><td>CLKIN</td><td>D／I</td><td>Clock input pin for external clock mode. Input clock frequency should be in a range of 10MHz±30% .</td><td>(4.3.3(2))</td></tr>
<tr><td>18</td><td>SSDT</td><td>D／I</td><td>Serial setting data input pin.
While SSCS is L level, the input SSDT data is synchronized to SCK and set to pre-setting register. The data load to control register at SSCS ascending timing, then new system setting is applied.</td><td rowspan="2">(4.3.1(2))</td></tr>
<tr><td>19</td><td>SSCS</td><td>D／I</td><td>Chip Select pin for serial input setting function. This signal control SSDT data reception and renewal system setting at ascending timing. If you do not use serial input function, please connect to VDD.<table><tr><th>SSDT Chip Select</th><th>Not accepted</th><th>Accepted</th></tr><tr><td>SSCS</td><td>H or Open</td><td>L</td></tr></table></td></tr>
<tr><td>20</td><td>DATA</td><td>D/O
(BUS)</td><td>Serial data output pin. When SCSB is L level, serial output data tansmit with synchronization to the SCK.</td><td rowspan="2">(4.3.2(2))</td></tr>
<tr><td>21</td><td>SCSB</td><td>D／I</td><td>Chip select pin for serial output function. This signal control DATA pin output mode and latch transmitting data when SCSB input falls down.<table><tr><th>DATA pin mode</th><th>Hi Impedance (Z)</th><th>Output</th></tr><tr><td>SCSB</td><td>H or Open</td><td>L</td></tr></table></td></tr>
<tr><td>22</td><td>PRTY</td><td>D/O
(BUS)</td><td>Even parity signal pin for output data(D0～D11). "H" level output signal number of D0～D11,PRTY must be even.</td><td></td></tr>
<tr><td>23</td><td>SCK</td><td>D／I</td><td>Serial Clock input pin. Use for serial input setting function and serial output function. Max frequency is 5MHz.</td><td>(4.3.1(2))
(4.3.2(2))</td></tr>
<tr><td>24</td><td>DGND</td><td>――</td><td>Digital ground pin. Connect to 0V.</td><td>(4.4)</td></tr>
</table>

(Note) "Class" means as follows.

＊A／I : Analog input　　＊D／I : Digital input

＊A／O : Analog output　　＊D／O(BUS) : Digital output(3-state output)

＊A／O(I) : Analog output/input(P13,P15 I/O are controlled by P1.)

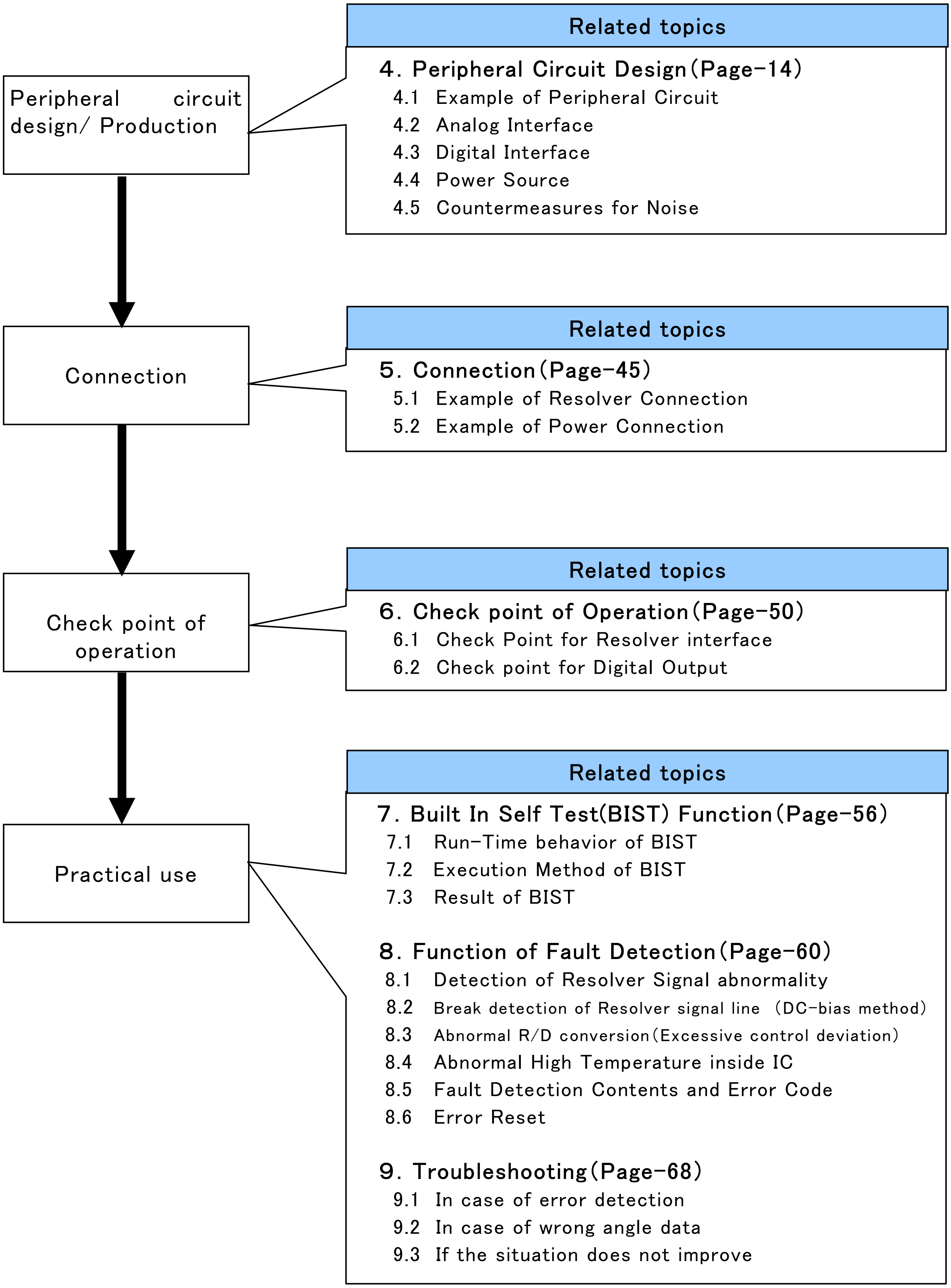
<table>
<tr><th>Pin No</th><th>Symbol</th><th>Class</th><th colspan="2">Description</th><th>Remarks chapter</th></tr>
<tr><td rowspan="2">25</td><td rowspan="2">D11</td><td rowspan="2">D/O(BUS)</td><td>Absolute output mode</td><td>Pulse output mode</td><td rowspan="13">(4.3.2(1))</td></tr>
<tr><td>φ1 (MSB)</td><td>ERRCD3</td></tr>
<tr><td>26</td><td>D10</td><td>D/O(BUS)</td><td>φ2</td><td>ERRCD2</td></tr>
<tr><td>27</td><td>D 9</td><td>D/O(BUS)</td><td>φ3</td><td>ERRCD1</td></tr>
<tr><td>28</td><td>D 8</td><td>D/O(BUS)</td><td>φ4</td><td>ERRHLD</td></tr>
<tr><td>29</td><td>D 7</td><td>D/O(BUS)</td><td>φ5</td><td>ERR</td></tr>
<tr><td>30</td><td>D 6</td><td>D/O(BUS)</td><td>φ6</td><td>—</td></tr>
<tr><td>31</td><td>D 5</td><td>D/O(BUS)</td><td>φ7</td><td>W</td></tr>
<tr><td>32</td><td>D 4</td><td>D/O(BUS)</td><td>φ8</td><td>V</td></tr>
<tr><td>33</td><td>D 3</td><td>D/O(BUS)</td><td>φ9</td><td>U</td></tr>
<tr><td>34</td><td>D 2</td><td>D/O(BUS)</td><td>φ10</td><td>Z</td></tr>
<tr><td>35</td><td>D 1</td><td>D/O(BUS)</td><td>φ11</td><td>B</td></tr>
<tr><td>36</td><td>D 0</td><td>D/O(BUS)</td><td>φ12 (LSB)</td><td>A</td></tr>
<tr><td>37</td><td>VDD</td><td>——</td><td colspan="2">Digital power pin.　Connect to +5V.</td><td>(4.4)</td></tr>
<tr><td>38</td><td>INHB(RD)</td><td>D／I</td><td colspan="2">Inhibit (Read) pin. This signal switch status(through/hold) for below corresponding signals.
■Pallarel output(D0～D11) and PRTY
・Absolute output mode ： φ1～φ12, PRTY
・Pulse output mode ： U, V, W, ERR, ERRHLD, ERRCD1～3
■Serial output
・Absolute output mode ： φ1～φ12, PRTY
・Pulse output mode ： U, V, W, ERR, ERRHLD, ERRCD1～3
・Result of BIST ： ERRHLD, ERRCD1～3
・Absolute out 16Bit mode ： φ1～φ16
<table><tr><th>Target output pin status</th><th>Through</th><th>Hold</th></tr><tr><td>INHB(RD)</td><td>H or Open</td><td>L</td></tr></table></td><td>(4.3.2)</td></tr>
<tr><td>39</td><td>ERRHLD</td><td>D／O(I)</td><td colspan="2">ERR(HOLD) pin. Once an abnormal condition is detected, this signal change to "H" and keep this status until activate error reset sequence.
This pin also serves as the default output mode setting for D0～D11. It is excuted by sensing the voltage level at power-up as an input pin., which has a pull-up resistor(10kΩ) or pull-down resistor(10kΩ).
<table><tr><th>D0～D11default setting</th><th>Absolute out mode</th><th>Pulse out mode</th></tr><tr><td>ERRHLD pin treatment</td><td>10kΩ pull-up</td><td>10kΩ pull-down</td></tr></table></td><td>(8),
(4.3.1(1))</td></tr>
<tr><td>40</td><td>ERRSTB</td><td>D／I</td><td colspan="2">Error reset pin. This signal reset ERRHLD and ERRCD1～3.
<table><tr><th>ERRHLD,ERRCD1～3 status</th><th>Hold</th><th>Clear(reset)</th></tr><tr><td>ERRSTB</td><td>H or open</td><td>L</td></tr></table></td><td>(8.6)</td></tr>
<tr><td>41</td><td>ERR</td><td>D／O(I)</td><td colspan="2">ERR output pin. While a error is detected, this pin output "H" level.
This pin also serves as the default output mode setting for operation clock. It is excuted by sensing the voltage level at power-up as an input pin., which has a pull-up resistor(10kΩ) or pull-down resistor(10kΩ).
<table><tr><th>Clock default setting</th><th>Internal oscillator</th><th>External clk input</th></tr><tr><td>ERR pin treatment</td><td>10kΩ pull-up</td><td>10kΩ pull-down</td></tr></table></td><td>(8),
(4.3.1(1))</td></tr>
<tr><td>42</td><td>A</td><td>D／O</td><td colspan="2">Equivalent to an encorder A pulse output pin.</td><td rowspan="2">(4.3.2(3))</td></tr>
<tr><td>43</td><td>B</td><td>D／O</td><td colspan="2">Equivalent to an encorder B pulse output pin.</td></tr>
<tr><td>44</td><td>Z</td><td>D／O(I)</td><td colspan="2">Equivalent to an encorder Z pulse output pin.
This pin also serves as the default output mode setting for excitation mode. It is excuted by sensing the voltage level at power-up as an input pin., which has a pull-up resistor(10kΩ) or pull-down resistor(10kΩ).
<table><tr><th>Excitation mode default setting</th><th>Current excitation</th><th>Voltage excitation</th></tr><tr><td>Z pin treatment</td><td>10kΩ pull-up</td><td>10kΩ pull-down</td></tr></table></td><td>(4.3.2(3))
(4.3.1(1))</td></tr>
<tr><td>45</td><td>CSB</td><td>D／I</td><td colspan="2">Chip select(CSB) pin.　This signal controls D0～D11、PRTY pins.
<table><tr><th>D0～11,PRTY pin mode</th><th>Hi Impedance</th><th>Data output</th></tr><tr><td>CSB</td><td>H</td><td>L</td></tr></table></td><td>(4.3.2(1))</td></tr>
<tr><td>46</td><td>PUPD</td><td>D／I</td><td colspan="2">This pin is an update frequency setting terminal of the parallel absolute value output.
<table><tr><th>Output update frequency setting</th><th>25MHz</th><th>12.5MHz</th></tr><tr><td>PUPD</td><td>H or open</td><td>L</td></tr></table></td><td>(4.3.1(3))</td></tr>
<tr><td>47</td><td>TEST1</td><td>D／I</td><td colspan="2">This is a test pin which is not directly involved in the operation.
Please treat it to short digital power supply (VDD) or open .</td><td></td></tr>
<tr><td>48</td><td>TEST2</td><td>D／I</td><td colspan="2">This is a test pin which is not directly involved in the operation.
Please treat it to short digital ground (DGND) or open .</td><td></td></tr>
</table>

(注) "Class" means as follows.

＊D／I ： Digital input　　＊D／O(I) ： Digital output(with internal pull-up for input)

＊D／O ： Digital output　　＊D／O(BUS) ： Digital output(3-state output)

3. Setup Flow


Peripheral circuit design/ Production
Connection
Check point of operation
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8.2 Break detection of Resolver signal line (DC-bias method)
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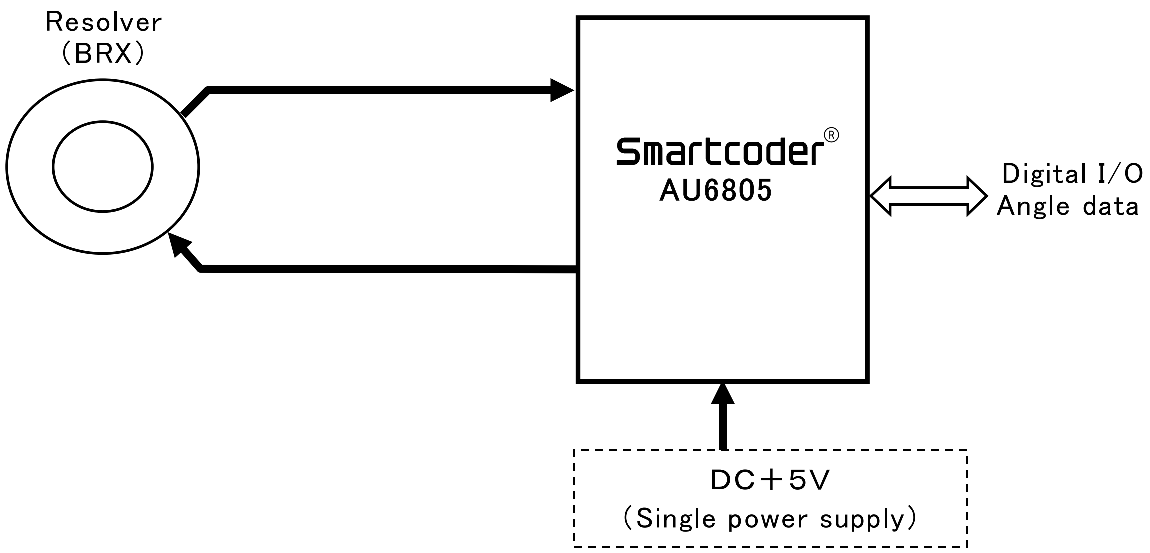
4. Peripheral Circuit Design

AU6805 require some peripheral circuit to get digital angle data. In this chapter, we explain the design method and important point for required peripheral circuit design.

4.1 Example of Peripheral Circuit



※ Some applications will require an external clock input and separate excitation amplifier.

4.2 Analog Interface

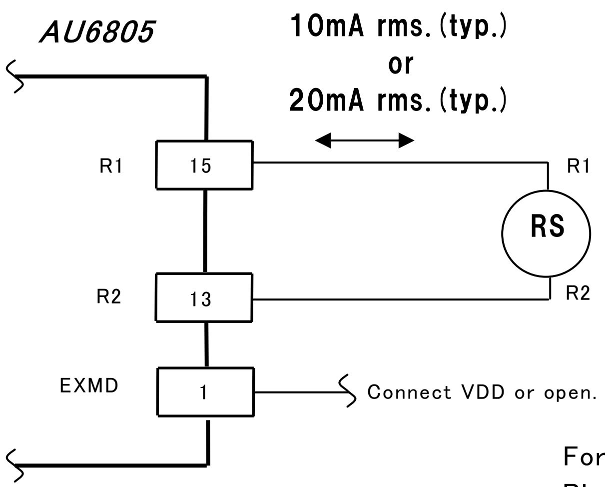
※ Examples mentioned in this articles shows only the concept of basic functions. Please note that each application might have their each individual requirement. Therefore the circuit configulation and the decision of constants for practical resistors and the function of protection for input/output circuits, etc. should be designed for each application by customer.

4.2.1 Resolver Excitation Circuit

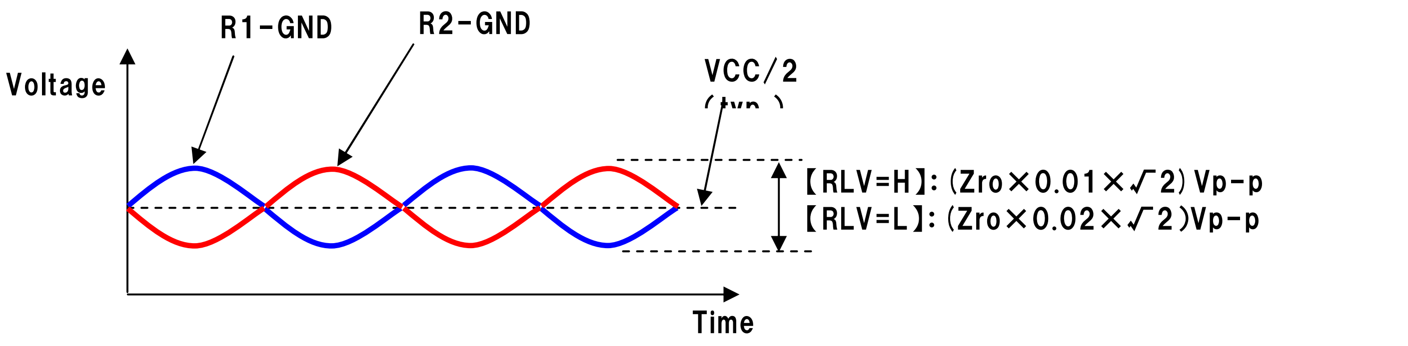
(1) Direct Excitation

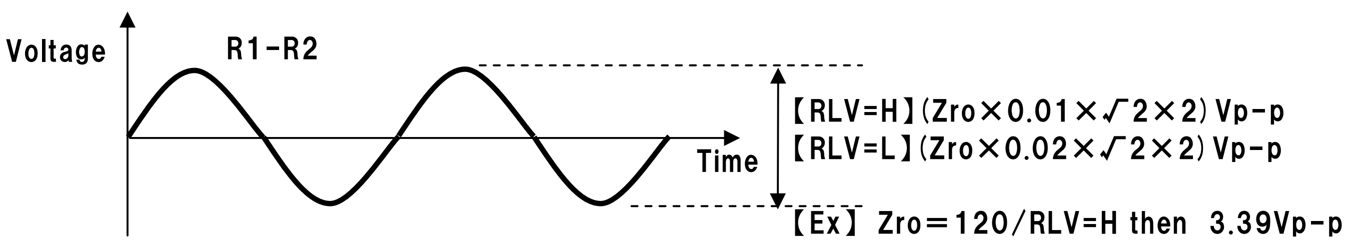
AU6805 has an excitation amplifier in the IC then it is possible to excite resolver directly. This excitation Amp is constant-current Amp, and current value can be select 10mArms.(typ.)/ 20mArms.(typ.) with RLV pin input setting. Without external amplifier system will make you possible to create cost-sensitive application system.

Note that the lower the input impedance value shows lower exciting voltage then it need noise considerations. In such case, exciting voltage booster amplifier might be prepared separately as shown in the following section.



For specific circuit configuration, Please refer P45.





(2) External excitation amplifier circuit

In case of severe noise environments, exciting voltage booster amplifier can be placed separately. There are 2 type of excitation amplifier circuit, current control type and voltage control type. Show merit/demerit of each method below. Please determine appropriate method for your system considering them.

Excitation Amp.	Merit	Demerit
Current control type	・Prevention of secondary failure(damage of output TR. Etc.) by short circuit between exciting lines. ・Resolver output fluctuations caused temperature change can be suppressed by a constant excitation current.	・Circuit is getting complex, and it might not operate as caliculations. ・Exciting voltage might vary due to resolver input impedance variability.
Voltage control type	・Circuit is simple and it will operate as caliculations. ・Exciting voltage can be constant.	・Possibility to have secondary failure due to overcurrent in case of short circuit between exciting lines. ・Easier to get the resolver output variation due to temperature changes.

Separate power supply (V_{EXT}) is required for the excitation amplifier circuit, in addition to the AU6805 +5V power supply.

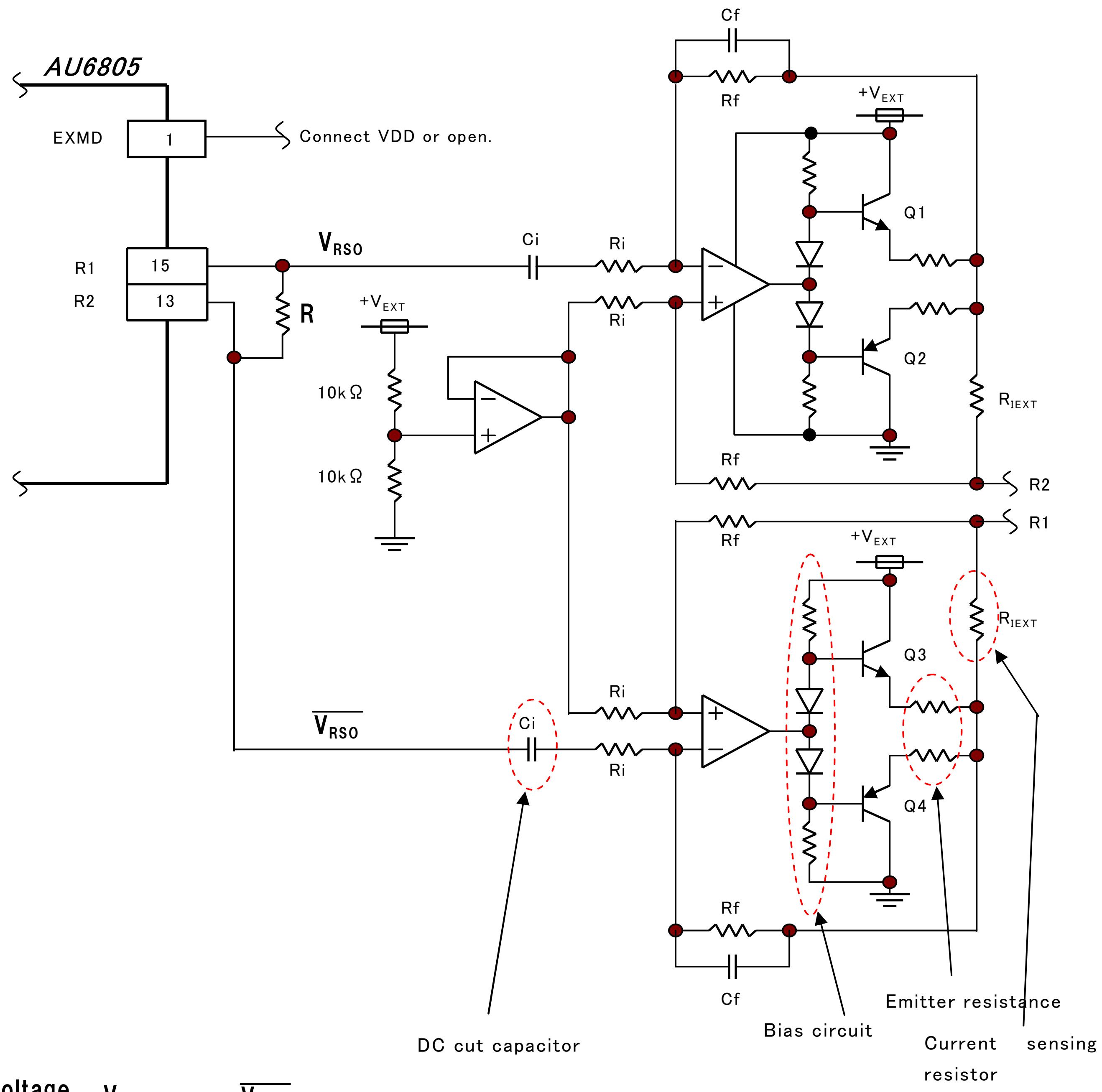
Higher resolver exciting voltage caused higher resolver output voltage and it can expect to improve the S/N ratio or noise immunity. That mean it need appropriate DC power supply. For example, exciting voltage 7Vrms (＝20Vp-p : $7V \times \sqrt{2} \times 2$) require ＋24V for single power source or ±15V for dual power sources.

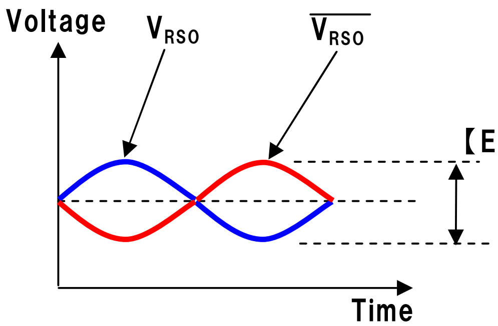
Resolver operation will be possible at the lower exciting voltage compared to the value described in the specification. So please decide exciting voltage value considering noise immunity and power equipment which can be prepared.

In this chapter, we will show you the example of excitation amplifier circuit (current control type) using AU6805 exciting output (R1,R2).

■Example circuit for single power source

①(Use general-purpose op-amp and push-pull circuit)





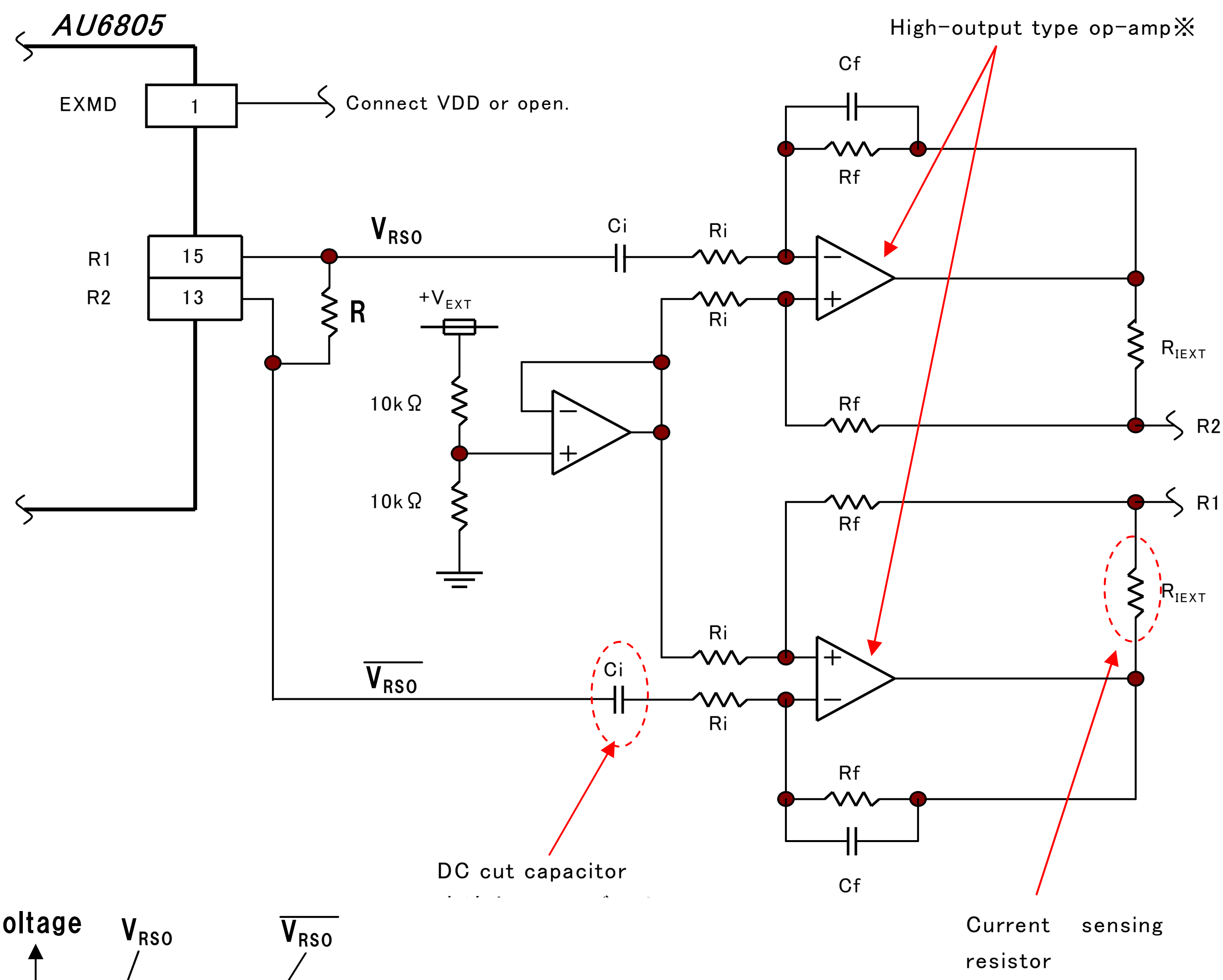
【Ex】 R＝150Ω, RLV=Hなら

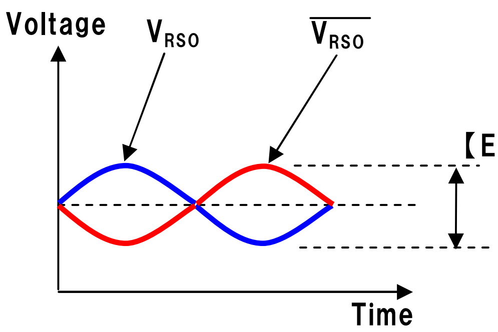
150×0.01×√2

＝2.12Vp-p

In case of V_{EXT} variation is expected by battery power, it must be defined standard operating at V_{EXT} minimum voltage.

■Example circuit for single power source
②(Use a high-output type op-amp)





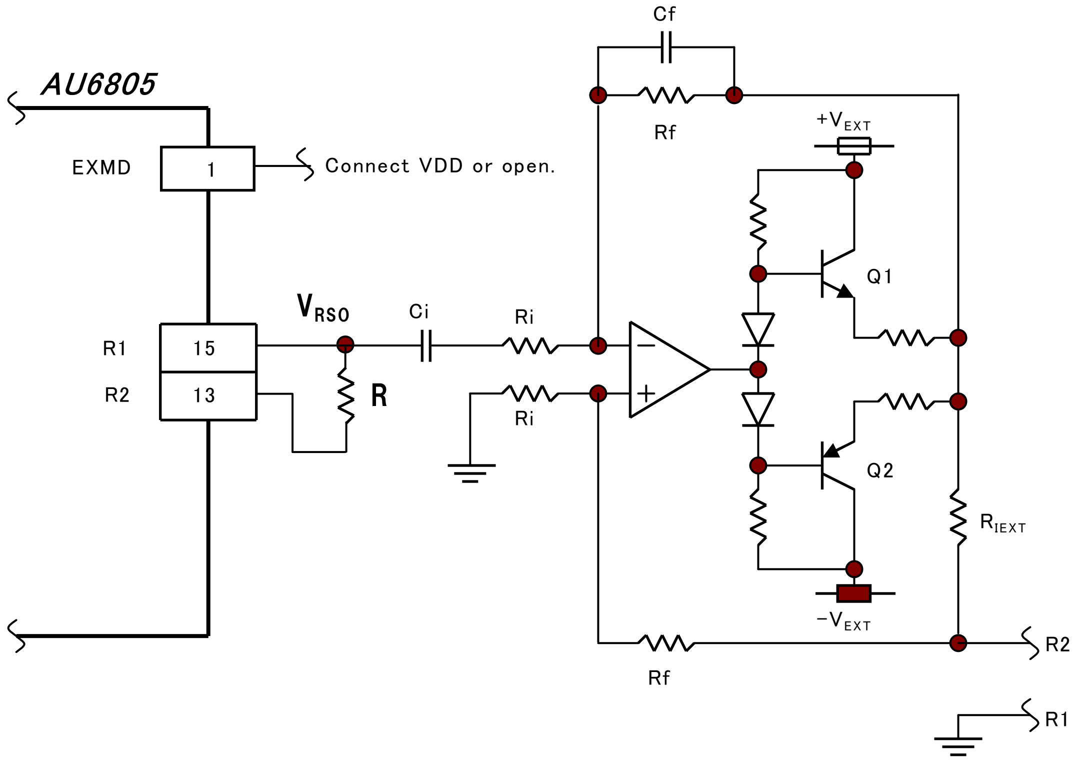
【Ex】 R=150Ω, RLV=H
150×0.01×√2
=2.12Vp-p

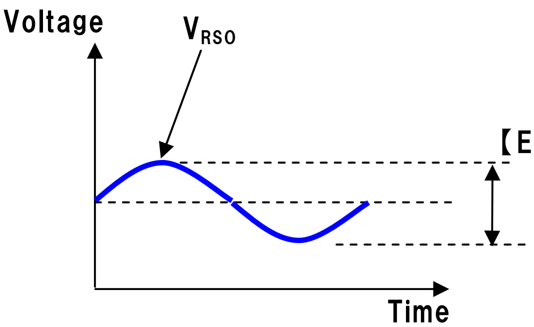
In case of V_{EXT} variation is expected by battery power, it must be defined standard operating at V_{EXT} minimum voltage.

※Example of High-output Op-amp is NJU77903(New Japan Radio Co., Ltd).
Contact the Op-amp manufacturers for details.

■Example circuit for dual power source

①(Use general-purpose op-amp and push-pull circuit)



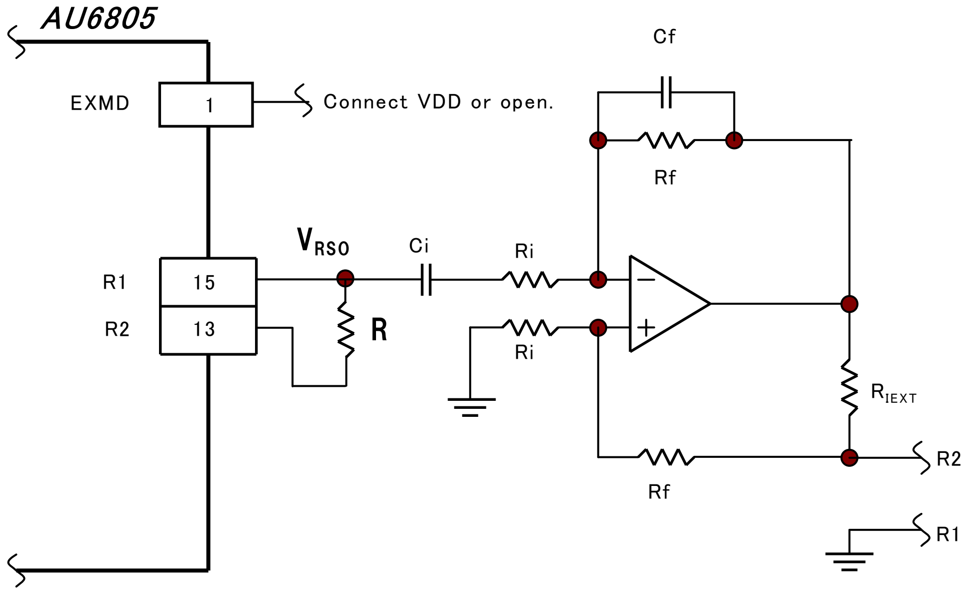


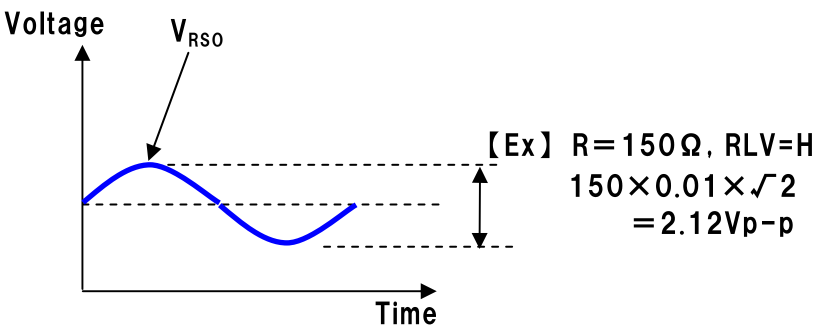
【Ex】 R＝150Ω, RLV=H

150×0.01×√2

＝2.12Vp-p

■Example circuit for dual power source
②(Use a high-output type op-amp)





※Example of High-output Op-amp is NJU77903(New Japan Radio Co., Ltd).
Contact the Op-amp manufacturers for details.

■Method for Setting constants of separate excitation amplifier(sample)

Refer below for setting constants.

≪Description of symbol≫

$+V_{EXT}$, $-V_{EXT}$: External power supply(For exciting voltage booster amplifier circuit)
I_{REF} : Exciting current of Resolver
R_{IEXT} : Resistor for setting exciting current of Resolver
V_{REF} : Exciting voltage of Resolver
Z_{RO} : Input impedance of Resolver(Specified value)
V_{RSO} : AU6805 R1 pin output voltage
R : Resistance between R1 pin and R2 pin(Current/Voltage conversion)
I_{RD} : AU6805 resolver exciting current (between R1pin and R2 pin)

Step① : Set the R1 terminal output voltage of AU6805.

$$V_{RSO} = I_{RD} \times R/2$$

Step② : Calculate the exciting current by setting the exciting voltage based on the voltage of external power supply.

$$V_{REF} = I_{REF} \times Z_{RO}$$

Step③ : Calculate the circuit constants based on the exciting current.

$I_{REF}/2 = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri)$ ·····For single power source

$I_{REF} = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri)$ ·····For dual power source

< Setting condition>

- I_{RD}=10mArms.typ【RLV=H】, I_{RD}=20mArms.typ【RLV=L】
- R≦200Ω【RLV=H】, R≦100Ω【RLV=L】
- $R_{IEXT} \leqq (Z_{RO}/10)$ [Ω]
- Rf≧50kΩ , Ci×Ri≧5×10^{-4} [s] , Cf×Rf≦5×10^{-6} [s]
- The power supply for an operational amplifier should be the same as that for the transistor buffer.

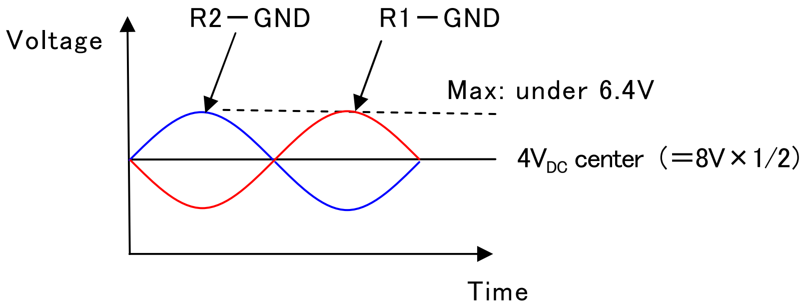
※This calculation method is based on DC circuit concept.
Resolver is a AC circuit and that input impedance (= R(RESISTANCE) +jX(CONDUCTOR)) cause voltage phase shift and current phase shift. Also there are some impacts at parallel connection of Rf and Cf. Then it might not get exact exciting voltage value as calculated.
In such a case, please adjust each constant by yourself. (Voltage can be adjusted by Ri value)
And it is effective to make pre-validation using circuit simulation like SPICE.

【Example】

V_{EXT}=Battery 12V(8V～16V fluctuation), Excitation frequency=10KHz,
Resolver Spec [Input impedance=76Ω (R-part:18Ω+L-part:1.18mH)]
Let's excite this resolver with current type amplifier described before.

V_{EXT} define as 8V(use minimum fluctuation).
Saturation voltage of OP-AMP assume as x0.8 supply. → 8V×0.8=6.4V

Regarding R1-GND and R2-GND,
Set amplitude center as $4V_{DC}$ (=8V×1/2)
Set amplitude as 4Vp-p
Then target amplitude is set as "R1-R2=8Vp-p".



Assumed I_{RD}=10mArms(RLV=H mode), and R=150Ω.

According to the formula of P21

AU6805 R1 pin output voltage(V_{RSO})= 2.12Vp-p (= 10mArms. × 150Ω×√2)
Exciting current of Resolver(I_{REF})=0.11Ap-p (=8Vp-p/76Ω)

R_{IEXT}=4.7Ω < Resolver input impedance(76Ω)/10
Rf=100kΩ
Then

$$I_{REF} = \frac{V_{RSO} \times Rf}{R_{IEXT} \times Ri \times 1/2}$$ ・・・・・For single power source

$$Ri = \frac{V_{RSO} \times Rf}{R_{IEXT} \times I_{REF} \times 1/2} = \frac{2.12Vp\text{-}p \times 100k}{4.7 \times 0.11 \times 1/2}$$

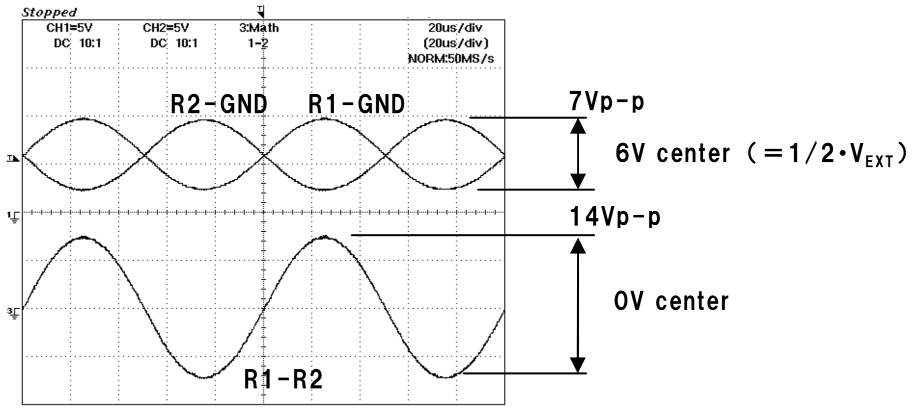
=820kΩ <---->

(Please adjust at actual circuit.)

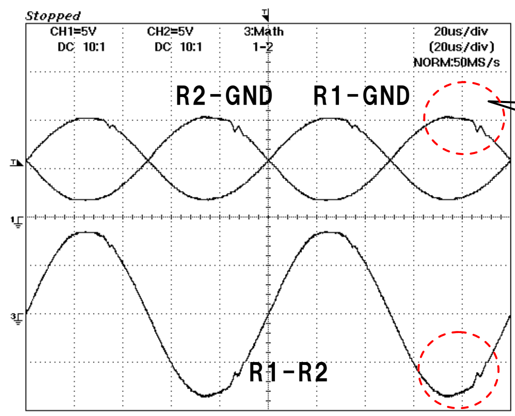
Example of circuit simulation,
Resolver input impedance
=18Ω+1.18mH
Cf =100p
Emitter resistance =4.7Ω
Bias resistance=1kΩ
Then around Ri = 560k Ω . (8Vp-p between R1-R2)

【Single power source V_{EXT}=12V waveform sample】

—Normal operation case—

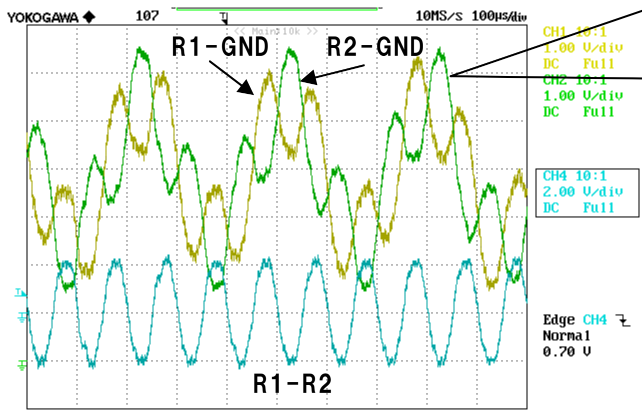


—Trouble (distortion case—

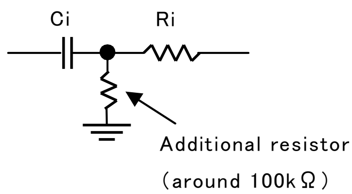


The wrong constant selection cause wider amplitude, and waveform distortion will be occurred by OP-AMP or Tr saturation voltage, etc.
Need to avoid distortion.

Rail to Rail OP-AMP type (saturation voltage is close to supply voltage) can set wider active output voltage without distortion generation.



It might happen to have R1-GND/R2-GND oscillation due to OP-AMP characteristic.
If this kind of wave is observed, DC cut Capacitor (Ci) might cause unstability of DC current. Then insersion of resistor between Ci output and GND will be effective to stabilize it.



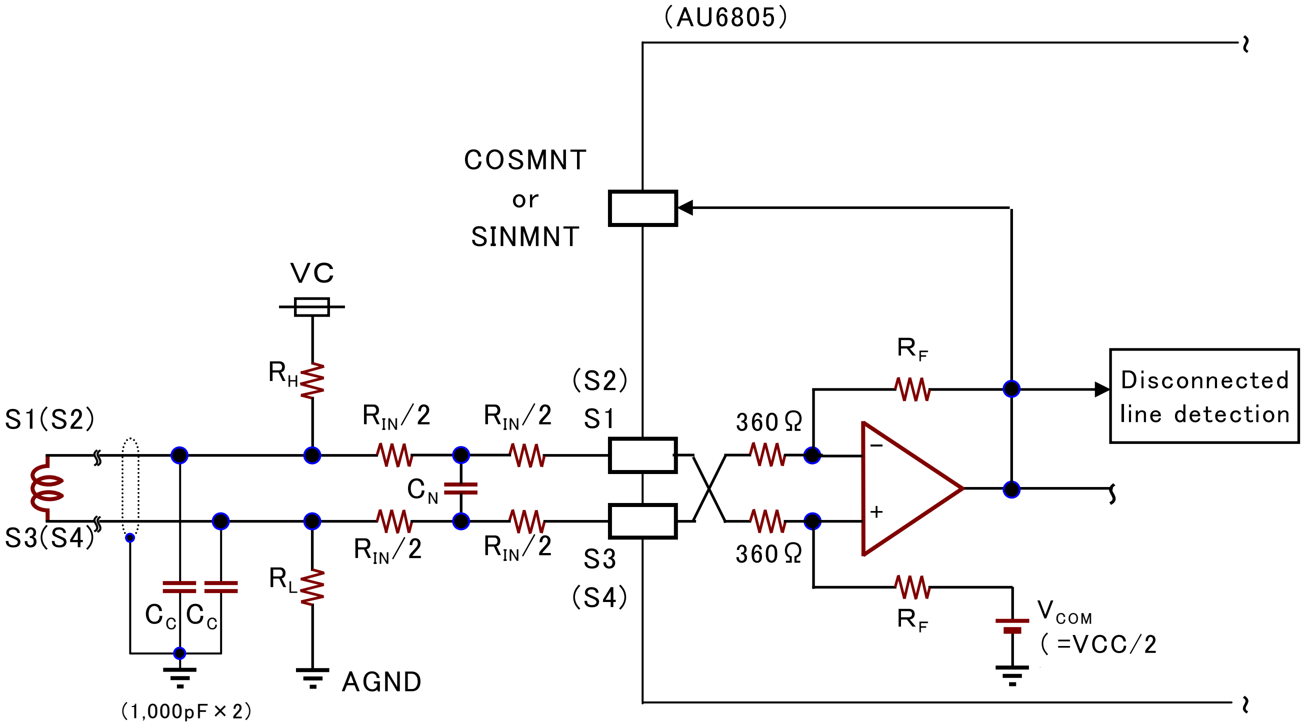
4.2.2 Resolver Signal Input Circuit

R/D conversion of AU6805will be done with monitor output(SINMNT, COSMNT). While voltage level of resolver signal is different with each application, it need to set appropriate monitor signal level with gain adjustment of resolver input signal to fit R/D conversion effectively. Also it need to have external DC bias resistor activating the function which detect any breaking of Resolver signal lines (S1~S4) mounted in AU6805.

In this chapter, show you example of resolver signal input circuit.

■Example of resolver signal input circuit

Below shows the Resolver Signal Input(Differential) Circuit < S1-S3, S2-S4 > and Monitor output equivalent circuit .



V_{COSMNT} , V_{SINMNT} : Resolver Signal Monitor Voltage
V_{COM} : Reference voltage of IC inside(=VCC/2)
R_F : 21kΩ±20%(Relative accuracy:±1%)

(Note) 1. Tolerance range【%】 of input resistance(R_{IN}) has impact to conversion accuracy[LSB]. 0.3% is equivalent to 1LSB.

2. Except the tolerance of input resistance and the performance of resolver itself, the variation of monitor output voltages(V_{SINMNT}, V_{COSMNT}) is within ±20% when resolver is directly excited by the AU6805 exciting output(R1 , R2).

(1) Gain setting resistor

The relationship between input resolver signal amplitude and monitor amplitude shows below.

$$\text{Monitor amplitude[Vp-p]} = \text{Resolver signal amplitude [Vp-p]} \times \frac{R_F}{R_{IN} + 360\Omega}$$

Gain setting resisitor R_{IN} value is defined as monitor MAX amplitude range 2～3Vp-p.

【Example】
Resolver spec (Exciting voltage: AC7Vrms, transformer ratio: 0.23),
Use it as exciting voltage 10Vp-p, and monitor output MAX amplitude assumed 2.5Vp-p.

Resolver output MAX＝2.3Vp-p （＝10Vp-p×0.23）より

$$2.5\ \text{Vp-p} = 2.3\ \text{Vp-p} \times \frac{21k\Omega}{R_{IN} + 360\Omega} \qquad \therefore R_{IN} = 19k\Omega$$

Note、asumed as $R_{IN} \geqq 2k\Omega$.

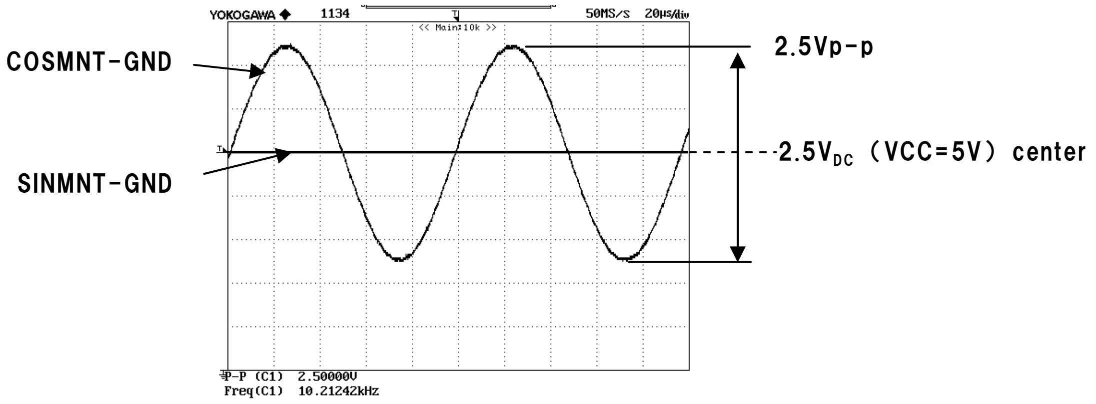
※If potential difference between SINMNT and COSMNT generate by the deviation of R_{IN}, it will caused error source. Please select appropriate resistor grade according to your required system tolerance.

［Example］ In case of there is a ＋Δ COSMNT against SINMNT,

$$\text{Error} = -\frac{1}{2} \cdot \Delta \cdot \text{SIN}2\theta \ \ \text{[rad]}$$

（Voltage difference 1% case: Δ＝0.01 Then Error max.＝±0.29°（＝±0.01/2 [rad]））

Example of monitor waveform （At 0°）



(2) DC bias resistor to detect breaking (R_H、R_L)

When the signal line break, monitor output level must be exceeded the threshold value and it need to set appropriate resistance value.

(1) $R_H \fallingdotseq \{(VCC - V_{COM}) / (12.5 \times 10^{-6})\} - R_{IN}$

(2) $R_L \fallingdotseq \{V_{COM} / (12.5 \times 10^{-6})\} - R_{IN}$ While $V_{COM} = VCC/2[V]$

Resistor value is determined in the range of 80~100% of the caliculated value.

In general、R_H 、R_L $= (180k\Omega - R_{IN}) \times (0.8 \sim 1.0)$

Without this DC bias resistor, fault detection depend on its angle (Could be detect at somewhere in rotation).

(Without this DC bias resistor, monitor output signal of breaking line will be about 0Vp-p. So when the normal monitor output side signal rotate to the position which is detected as fault range of Rsolver signal abnormality, fault can be detect.)

※ (To customers who have experience to use AU6802N1.)
Please note that the connection polarity of a DC bias resistors (RH,RL) are different (reverse) with AU6802N1 connection.

(3) Normal mode capacitor (C_N)

While basic circuit shouldn't have C_N, it can improve electorical noise.

Cause the gain resistor(R_{IN}) and C_N work as filter, it will be one of the factor of phase shift.

Time constant $= 2 \times ((R_{IN}/2) // (R_{IN}/2)) \times C_N$

※ $(R_{IN}/2)//(R_{IN}/2)$ means parallel connection resistance value of $(R_{IN}/2)$ and $(R_{IN}/2)$.

This capacitor has an impedance$\{=1/(\omega \cdot C_N)\}$ and it affect signal level also.
Deviation of capacitor is much worse than that of resistor, please select the small deviation parts or small capacitance part to avoid impact of signal level.

(4) Common mode capacitor (C_C)

Standard usage is putting 1000p capacitor between S1~S4 signal and GND.

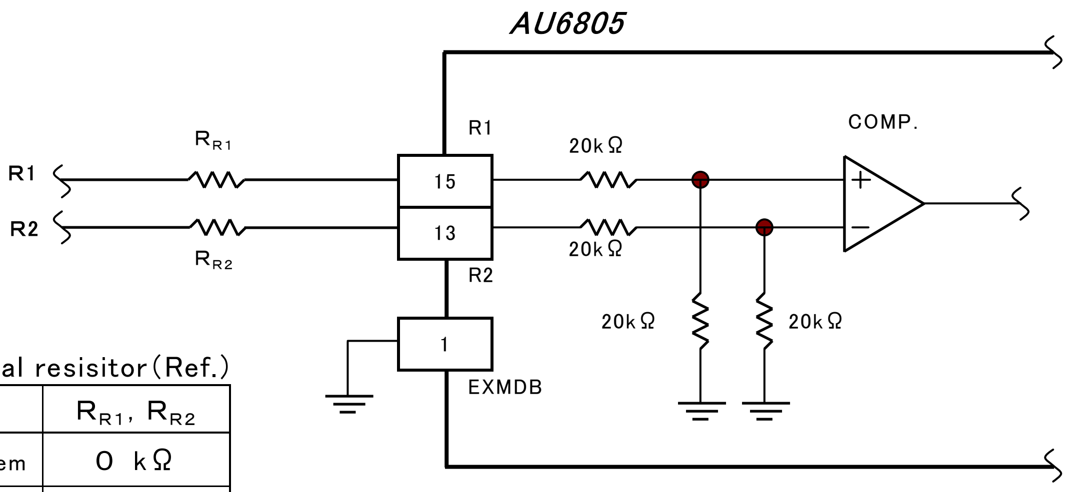
4.2.3 External input circuit for resolver (External excitation case)

※This chapter shows an example input circuit when you use external excitation source.
You do not need to prepare these resolver excitation input circuit, while your resolver excite with this product R1/R2 output directly or you implement external amplifier with this product R1/R2 signal source.

In case of applying external excite source, AU6805 R/D conversion require synchronous detection function which use a phase signal with the external input (R1, R2) of resolver excitation signal. Then R1/R2 input needs to have same phase input signal with the carrier of resolver signal. In this chapter, there shows example external input circuit of resolver excitation signal.

※When you use external excitation source, AU6805 EXMDB pin must set as "L" level, It mean that R1/R2 terminal must be input mode setting.

(1)Basic circuit sample (using single power source for external excitation source)

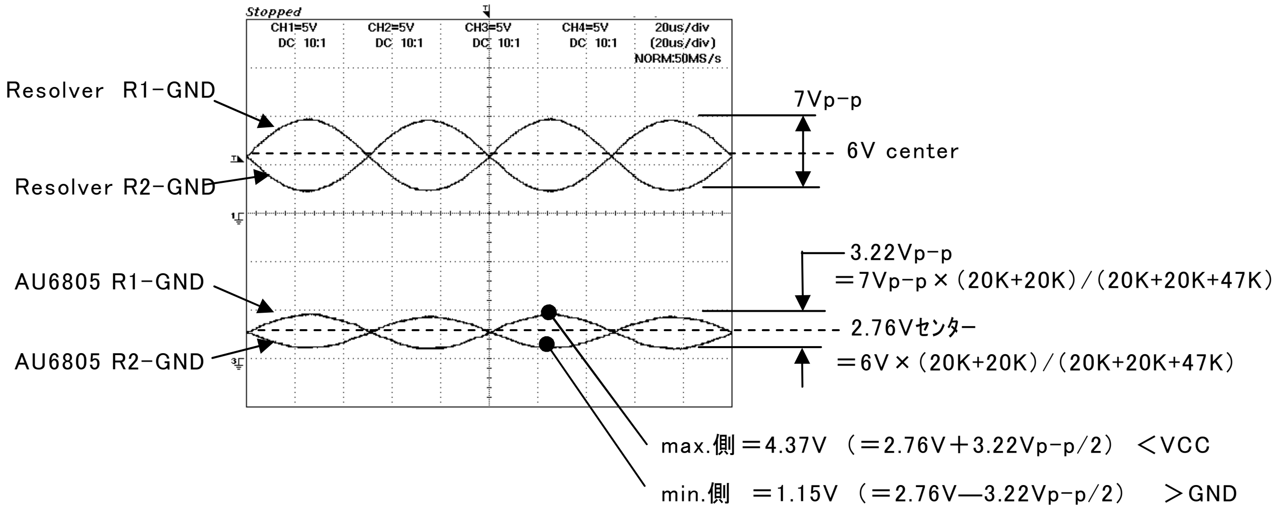


External resisitor(Ref.)

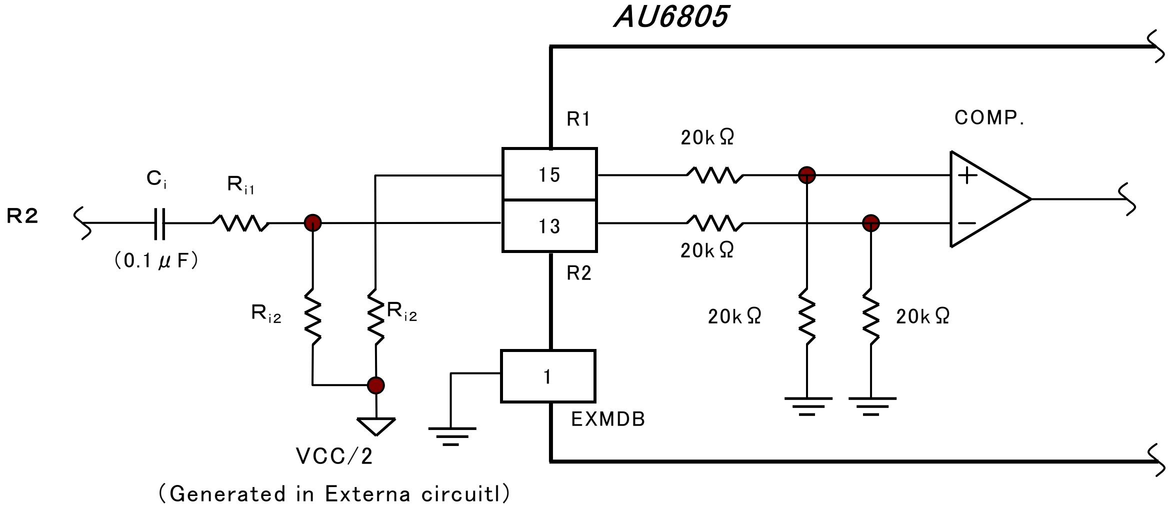
VEXT	R_{R1}, R_{R2}
+5V system	0 kΩ
+12Vsystem	47 kΩ
+24Vsystem	120 kΩ

In case of direct input for AU6805 R1/R2 terminals, exciting signal level might exceed VCC and it cause some failure. So please note that the terminal voltage for AU6805 R1/R2 should not exceed VCC(Power supply voltage) by means of adding the external resistor(R_{R1}、R_{R2})to divide the voltage.

R_{R1}, R_{R2}＝47KΩ example



(2)Basic circuit sample (using dual power source for external excitation source)



In this dual power source case, an exciting signal is 0V center. So it needs to make AU6805 R1/R2 terminal input level as shifting DC level. There might happen to exceed 0V˜VCC range of AU6805 R2 terminal voltage, and it cause some failure. Then the terminal voltage for AU6805 R2 should not exceed 0V˜VCC by means of adding the external resisitor (R_{i1}、R_{i2})to divide the voltage.

DC cut Capacitor(Ci)＞0.1μ

R_{i2}= around 3.3～4.7KΩ (around 10% of (20KΩ＋20KΩ))

$$\text{Center value of swing [V]} = \text{VCC/2 [V]} \times \frac{20K + 20K}{20K + 20K + R_{i2}}$$

$$\text{Amplitude level [Vp-p]} = \text{R2 [Vp-p]} \times \frac{R_{i2}}{R_{i1} + R_{i2}}$$

Waveform max. value＝(Center of swing)＋(Amplitude level)/2 ＜ VCC

Waveform min. value＝(Center of swing)－(Amplitude level)/2 ＞ 0V

【Example】

Assuming resolver R2＝10Vp-p.

And also assuming R_{i2}＝4.7K

Center value of swing ＝2.5V × $\frac{20K + 20K}{20K + 20K + 4.7K}$ ＝2.24V

Assuming 3Vp-p for AU6805 R2 terminal amplitude level.

3 [Vp-p]＝10 [Vp-p] × $\frac{4.7K}{R_{i1} + 4.7K}$ ∴R_{i1}＝10.9K→11K

Waveform max. value＝2.24V+3V/2=3.74V ＜VCC "OK"

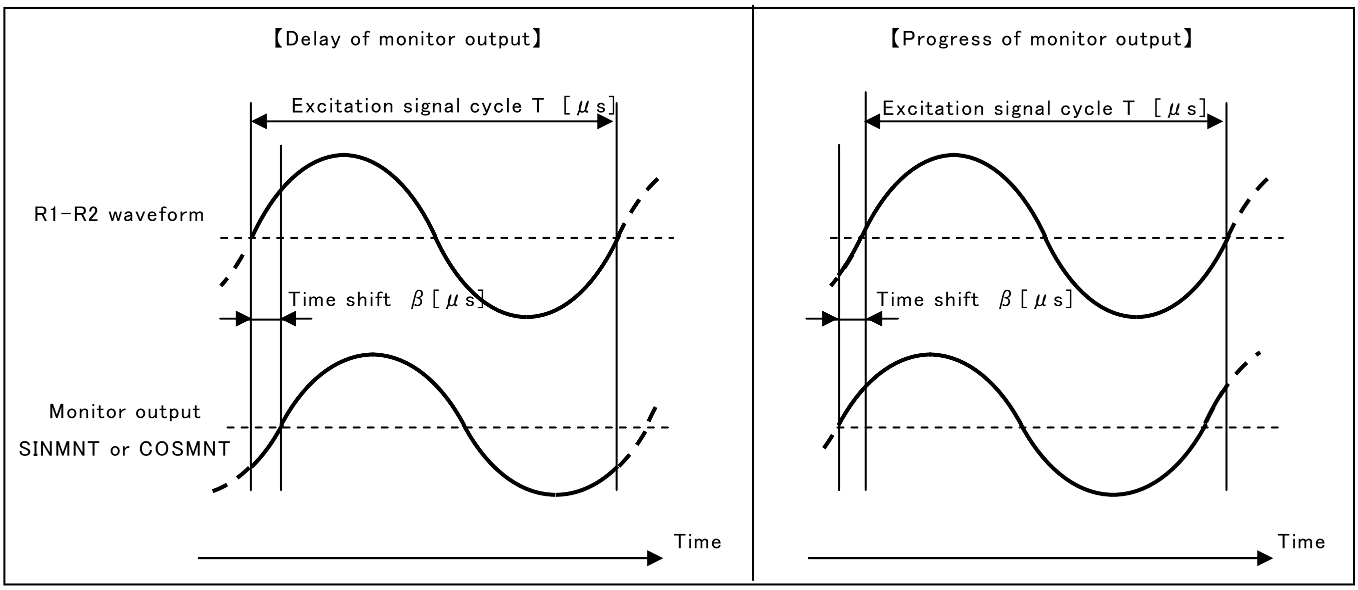
Waveform min. value＝2.24V－3V/2=0.74V ＞0V "OK"

(3) Considering the phase shift

Even if there is phase difference between AU6805 monitor output signal and external exciting signal input(R1-R2), AU6805 can operate automatical phase correction in case of phase difference is under ±45°. Normally there is no need for consideration of phase correction.

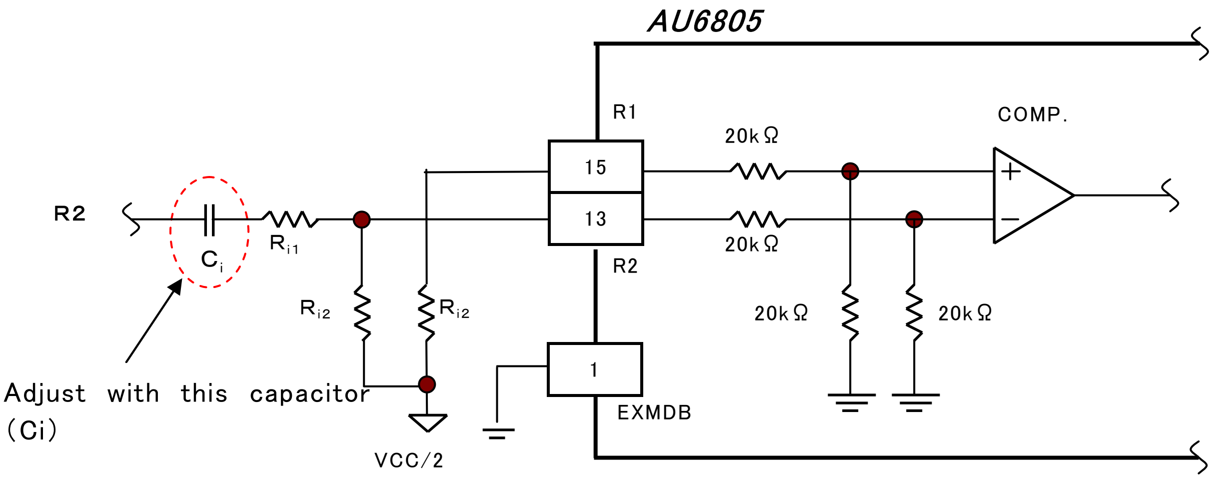
However in case of over 45° phase difference, the loop gain of R/D conversion system will be equivalently decreased. It means that R/D conversion spent long time to settle down the angle output or not to be able to settle down the angle data. In such case, a phase adjustment circuit can be inserted into the R1/R2 input to adjust difference value under ±45°.

■How to get converted angle from phase shift value.



Phase shift angle (α) corresponding value (°) $= \frac{\beta}{T} \times 360^\circ$

① How to adjust progressing phase



There might happen to exceed 0V~VCC range of AU6805 R2 terminal voltage, and it cause some failure. Then the terminal voltage for AU6805 R1/R2 should not exceed 0V~VCC range by means of adding the external resistor (R_{i1}、R_{i2}) to drive the voltage.

■The amount of progressing phase (indication)

"The amount of progressing phase" $\alpha = \arctan\left\{\frac{1}{2\pi \times f \times C_i \times (R_{i1} + R_{i2})}\right\}$ [degree]

【Example】
When R2=10Vp-p, would like to set 40° for progressing phase.
(excitation frequency=10KHz)

※ R_{i1}、R_{i2} concept is same as chapter 4.2.3 (2).

Assuming R_{i1}=11K、R_{i2}=4.7K,

$$40° = \arctan\left\{\frac{1}{2\pi \times 10000 \times C_i \times (11K + 4.7K)}\right\}$$

$$C_i = \frac{1}{2\pi \times 10000 \times (11K + 4.7K) \times \tan 40°}$$

=0.00121μ → 0.0012μ
(Please adjust it with actual circuit.)

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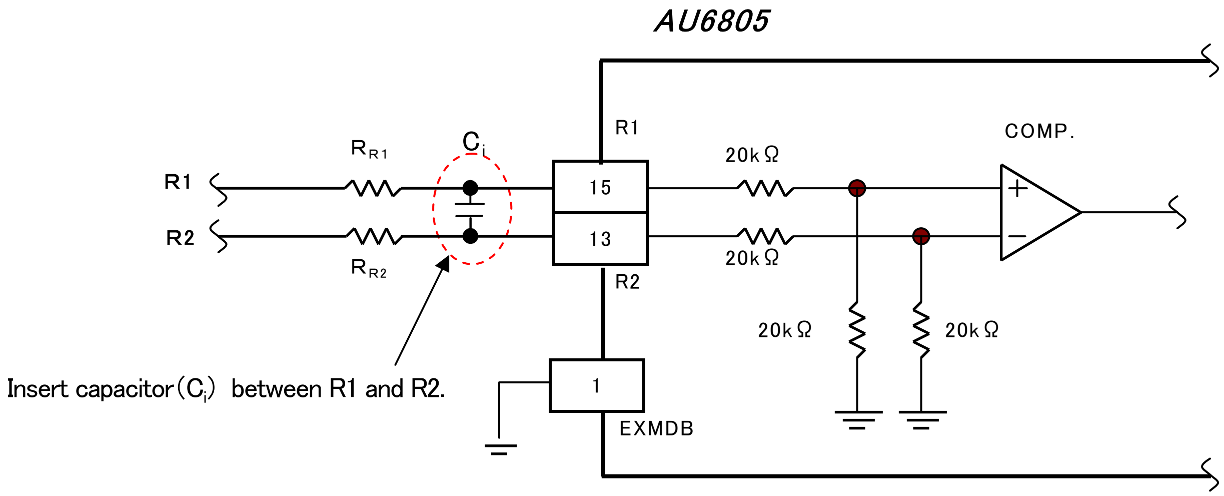
②How to adjust delaying phase

②-1 Basic circuit to adjust delaying phase
(Use single power source for exciting amplifier)



■The amount of progressing phase (indication)

"The amount of progressing phase" $\alpha = \arctan[2\pi \times f \times C_i \times 2 \times (R_{R1} // (20K+20K))]$ [degree]

※"R_{R1}//(20K+20K)" means parallel connection resistor value of R_{R1} and (20K+20K).

【Example】
When R_{R1}、R_{R2}=47K, would like to set 40° for delaying phase
(excitation frequency=10KHz)

R_{R1}//(20K+20K)=21.6KΩ

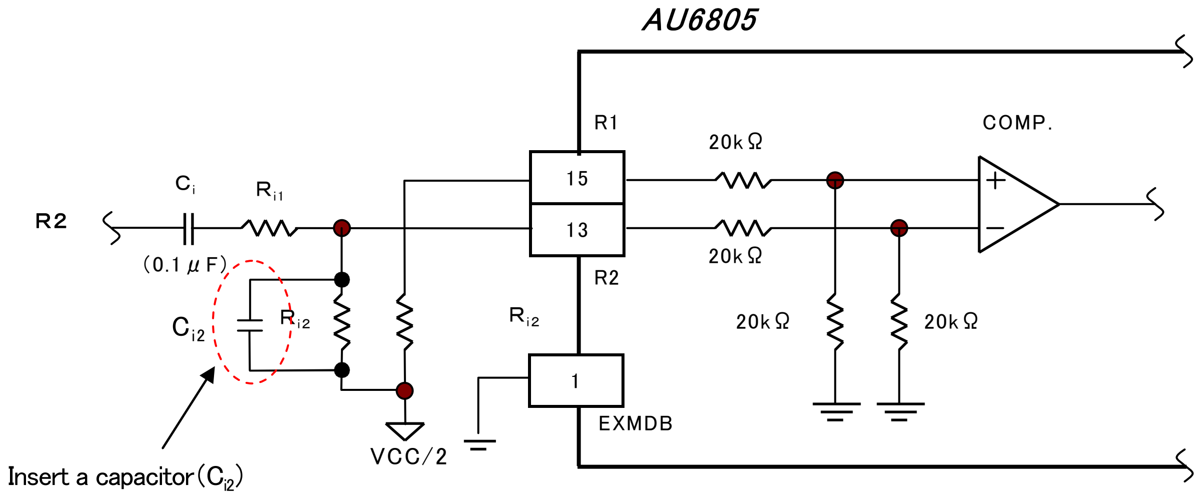
$$40° = \arctan(2\pi \times 10000 \times C_i \times 2 \times 21.6K)$$

$$C_i = \frac{\tan 40°}{2\pi \times 10000 \times 2 \times 21.6K}$$

=309p → 330p
(Please adjust it with actual circuit.)

②-2　Basic circuit to adjust delaying phase

(Use dual power source for exciting amplifier)



■The amount of progressing phase(indication)

"The amount of progressing phase"　$\alpha = \arctan[2\pi \times f \times C_{i2} \times (R_{i1} // R_{i2})]$　[degree]

※($R_{i1}//R_{i2}$) means parallel connection resistor value of R_{i1} and R_{i2}.

【Example】

When R2=10Vp-p, would like to set 50°.

(excitation frequency=10KHz)

※R_{i1}、R_{i2} concept is same as chapter 4.2.3 (2).

Assuming R_{i1}=11K、R_{i2}=4.7K .

$R_{i1}//R_{i2}$=3.3KΩ

$$50^\circ = \arctan(2\pi \times 10000 \times C_{i2} \times 3.3K)$$

$$C_{i2} = \frac{\tan 50^\circ}{2\pi \times 10000 \times 3.3K}$$

=5748p → 5600p

(Please adjust it with actual circuit.)

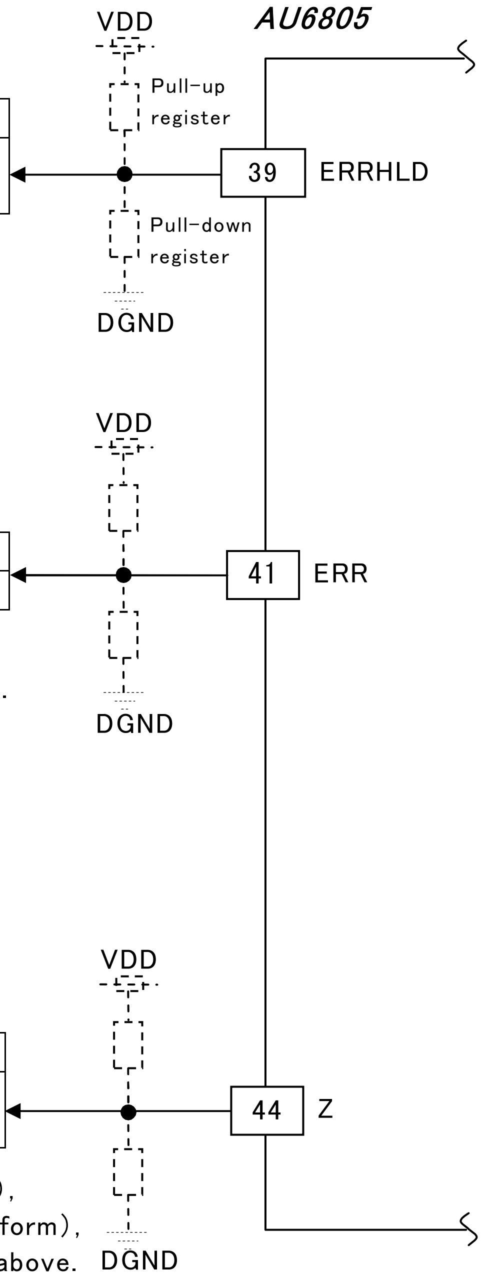
4.3 Digital Interface

4.3.1 Mode Setting・Function Selection

(1) Default setting

AU6805 has a mode-setting function that detects the terminal voltage level as an input terminal at power-on, by means of adding a pull-up register of 10KΩ or a pull-down register of 10KΩ to the output terminals.

Please make the appropriate settings for each application in this function.



■Output-mode setting

	Pull-up (10kΩ)	Pull-down (10kΩ)
Output mode (D0−D11)	Absolute parallel angle data	Pulses equivalent to encoder

Parallel out pins (D0−D11) mode setting.
Refer section 2.2、4.3.2(1) for actual description.
(Serial output is not covered by this setting.)

※This setting can be rewritten in the serial input configuration.
(Target setting register: Bit 1)

■Oscillator selection for excitation

	Pull-up (10kΩ)	Pull-down (10kΩ)
Oscillator	Internal oscillator	External clk input

Select the source of excitation output.
Internal oscillator: The IC's internal oscillator is used.
External clk: Use an external clock input.

Excitation frequency= Clk_frequency/1000

※This setting can be rewritten in the serial input configuration.
(Target setting register: Bit 2)

■Excitaion output mode setting

	Pull-up (10kΩ)	Pull-down (10kΩ)
Excitation mode	Current excitation mode (VMD=0)	Voltage excitation mode (VMD=1)

Reference waveform (Current waveform between R1-R2), and Resolver signal input (SINMNT, COSMNT pin waveform), Select appropriate mode by checking phase difference of above.

■Phase difference=+90° ±45° -→ Current excitation mode (VMD="0")
■Phase difference= 0° ±45° -→ Voltage excitation mode (VMD="1")

※If this mode setting is incorrect, AU6805 can not make correct R/D conversion.
※This setting can **NOT** be rewritten in the serial input configuration.

(2) Serial input setting

AU6805 has a function that makes it possible to change the contents of the setting register shown in below table through the serial input. At this function, it is possible to set right operation mode for individual applications, and set the content in diagnostic of BIST function.

※The "SSCS" input terminal should be connected to the power supply(VDD) when this function is not used.
※Setting register contents changed by this function will be held until the configuration change is made again.
In case of power shut-down or system-reset(re-boot), register configuration reset to 4.3.1(1) setting.

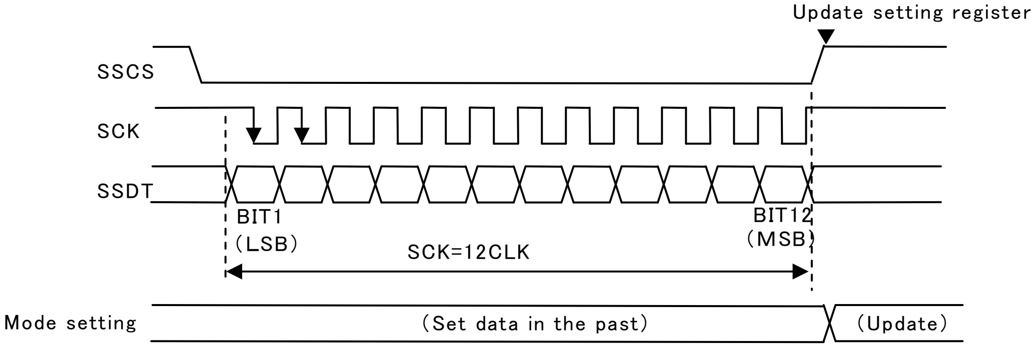
■Description of serial input setting register

<table>
<tr><th>Bit NO.</th><th>Item</th><th colspan="3">設 Description of setting</th></tr>
<tr><td>1</td><td>Output Mode Setting
(D0～D11)</td><td colspan="3">[0] : Absolute-value(φ1～φ12)Parallel Angle Data
[1] : Equivalent Encorder Pulse(A,B,Z,U,V,W)</td></tr>
<tr><td>2</td><td>Selection of
Exciting clock</td><td colspan="3">[0] : Internal Oscillator
[1] : External Clock Input</td></tr>
<tr><td>3
4</td><td>Serial Output
Mode Setting
[Bit 4,3]</td><td colspan="3">[00] : Absolute-value(φ1～φ12)Angle data
[01] : Equivalent Encorder Pulse(A,B,Z,U,V,W)
[10] : Serial Callback(Setting Register Confirmation)
[11] : Failure Detection／BIST result</td></tr>
<tr><td rowspan="5">5
6</td><td rowspan="5">Loop gain setting
[Bit 6,5]</td><td></td><td>Loop gain setting group A
[Bit 11]=[0]</td><td>Loop gain setting group B
[Bit 11]=[1]</td></tr>
<tr><td>[00]</td><td>Fixed value①
(Bandwidth 800Hz(typ.))</td><td>Fixed value⑤
(Bandwidth 1,000Hz(typ.))</td></tr>
<tr><td>[01]</td><td>Fixed value②
(Bandwidth 2,000Hz(typ.))</td><td>Fixed value⑥
(Bandwidth 500Hz(typ.))</td></tr>
<tr><td>[10]</td><td>Fixed value③
(Bandwidth 2,500Hz(typ.))</td><td>Fixed value⑦
(Bandwidth 200Hz(typ.))</td></tr>
<tr><td>[11]</td><td>Fixed value④
(Bandwidth 1,500Hz(typ.))</td><td>Loop gain Auto tuning
(Bandwidth 220Hz～460KHz
(typ.) automatic adjustment)</td></tr>
<tr><td>7
8
9
10</td><td>BIST
(Built In Self Test)
Setting
&
Special mode
setting
[Bit 10,9,8,7]</td><td colspan="3">[0000] : BISTVLD(Input) Invalid
[0001] : Reserved(Do not use)
[0010] : Reserved(Do not use)
[0011] : Reserved(Do not use)
[0100] : Reserved(Do not use)
[0101] : Angle convert BIST:Angle-1(0°)
[0110] : Angle convert BIST:Angle-2(45°)
[0111] : Angle convert BIST:Angle-3(270°)
[1000] : Reserved(Do not use)
[1001] : Failure detection BIST:resolver signal abnormality BIST
[1010] : Failure detection BIST:Signal break BIST(COS side)
[1011] : Failure detection BIST:Signal break BIST(SIN side)
[1100] : Failure detection BIST:conversion abnormality BIST
[1101] : System reset(Re-boot)
[1110] : Serial Absolute-value Output 16 BIT Mode
[1111] : Reserved(Do not use)</td></tr>
<tr><td>11</td><td>Loop gain setting
Group selection</td><td colspan="3">[0] : Group A(＊Refer to Loop gain setting[Bit6,5])
[1] : Group B(＊Refer to Loop gain setting[Bit6,5])</td></tr>
<tr><td>12</td><td>Threshhold selection
for signal abnormality</td><td colspan="3">[0] : 0.1×VCC[Vp-p]
[1] : 0.14×VCC[Vp-p]</td></tr>
</table>

※Setting default value is [0] in all BIT except default setting mentioned at 4.3.1(1) .

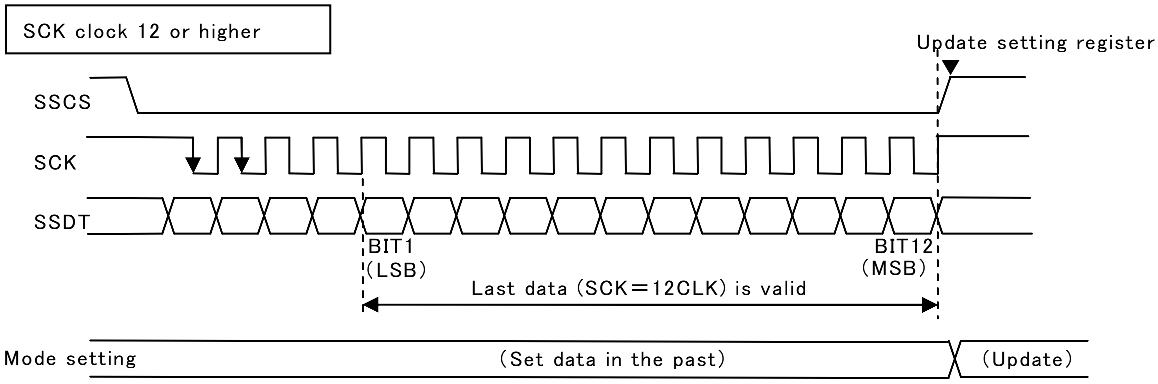
■Setting method

Serial input operation is controlled by SSCS/SCK/SSDT pins. SSDT data will be entered by synchronized timing to SCK input at the active condition of SSCS input "L" level. Please switch the SSDT input at the rising edge of SCK, while SSDT data will be incorporated at the falling edge of SCK.

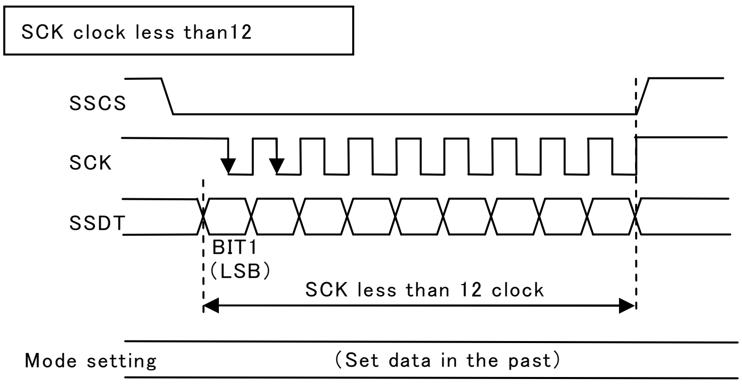


※Refer 10.9 to check each signal timing.

Note, when SCK clock number is greater than 12 while SSCS="L", effective data will be last 12 one of the last 12 SCK.

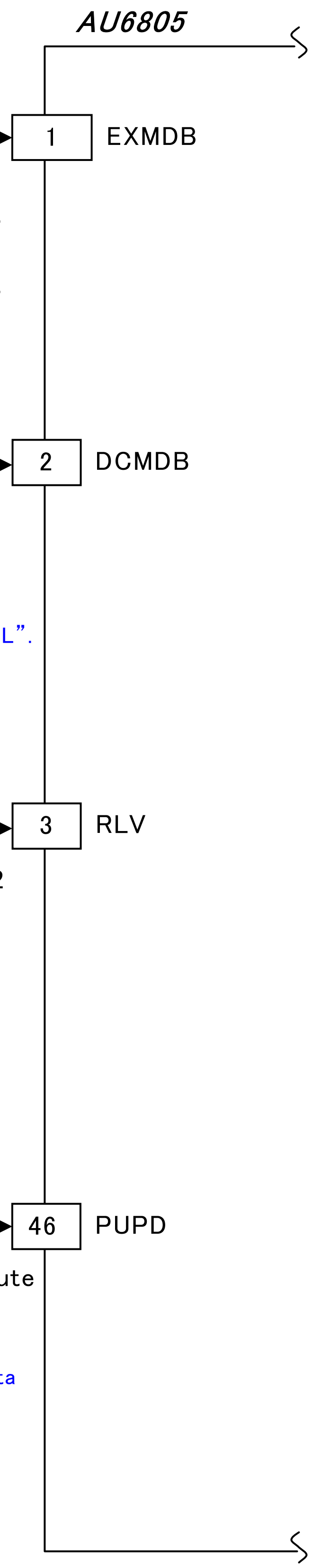


(Note) When SCK clock number is less than 12 while SSCS="L", input data is invalid and control register is not updated.



(3)Digital input setting

AU6805 has a function that allows you to set up by the digital input terminals, except for default setting and serial input setting. It include “R1/R2 I/O switching”, “sensor selection”, “Exciting current selection”, and “parallel absolute output update time selection”.



■R1/R2 Input/Output switching

R1,R2 pin	Exciting current out	Exciting signal input
EXMDB	“H”	“L”

R1/R2 pin I/O setting.
Exciting current out: Use AU6805 exciting output for rsolver exciting.
Exciting signal input : Use external exciting source for resolver exciting.

■Sensor selection

Sensor signal form	resolver	DC resolver
DCMDB	“H”	“L”

Selection of sensor signal form to be used.
Resolver: BRX resolver signal(AC signal)
DCレゾルバ:SIN/COS signal without carrier(DC signal)

※EXMDB setting is valid(higher priority) when both EXMDB/DCMDB are “L”.

■Exciting current selection

Current value	10mArms.(typ.)	20mArms. (typ.)
RLV	“H”	“L”

Make a selection of the output current value when R1/R2 terminals set as exciting current output mode.

■Parallel absolute output update time selection

Update freq.	25MHz(typ.)	12.5MHz(typ.)
PUPD	“H”	“L”

Make a selection of data update frequency for parallel absolute angle data.

※This setting affect only parallel absolute angle data. Other output data do not change update frequency.

4.3.2 Output Interface

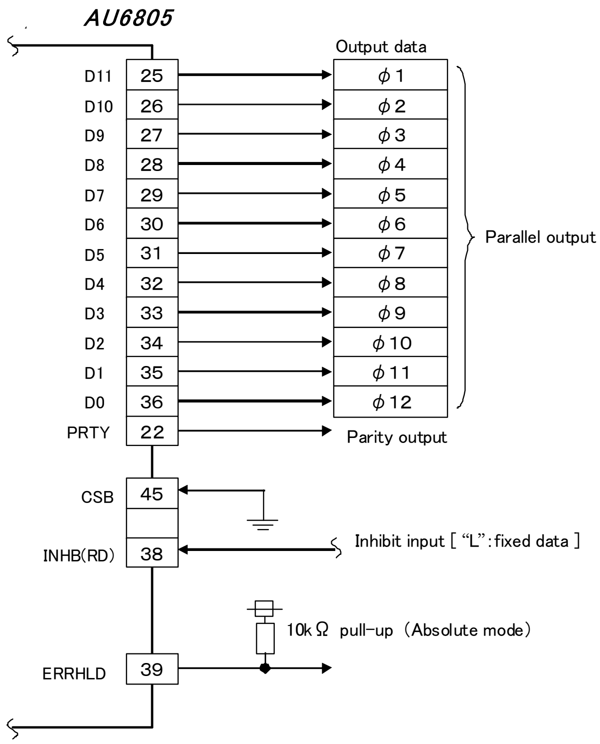
(1)Parallel output

Examples of parallel output are as follows. Note that it assumed to make parallel output mode setting by default setting (refer 4.3.1(1)) in this chapter. It is also OK to use serial input setting (refer 4.3.2(2)).

■ Usage of Absolute output mode

—《stand-alone》 usage : Interfaced by dedicated I/O—

When it use in standalone, CSB pin must be "L" lebel. And please read "ϕ1˜ϕ12" data which control through/hold by INHB(RD) pin.

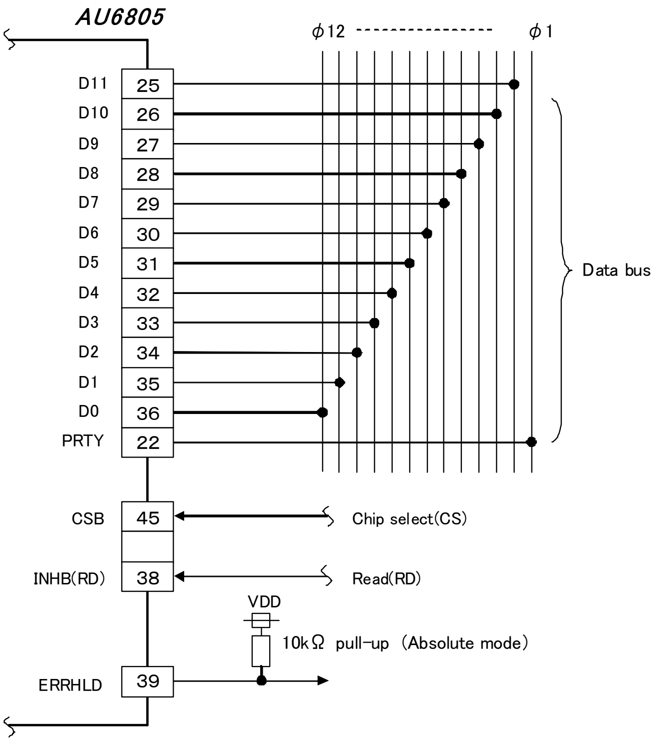


※ Please refer chapter 10.9 for ϕ1～ϕ11、PRTY、CSB、INHB timing.

(Note) PRTY is an even parity output. The number of single digit will be even while data include parallel ϕ1～ϕ12 and PRTY.

—《Bus interface》 usage ： Interfaced by BUS line—

When it use in bus line, D0～D11 and PRTY output state must be controlled by CSB pin. And please read "ϕ1~ϕ12" data which control through/hold by INHB(RD) pin.

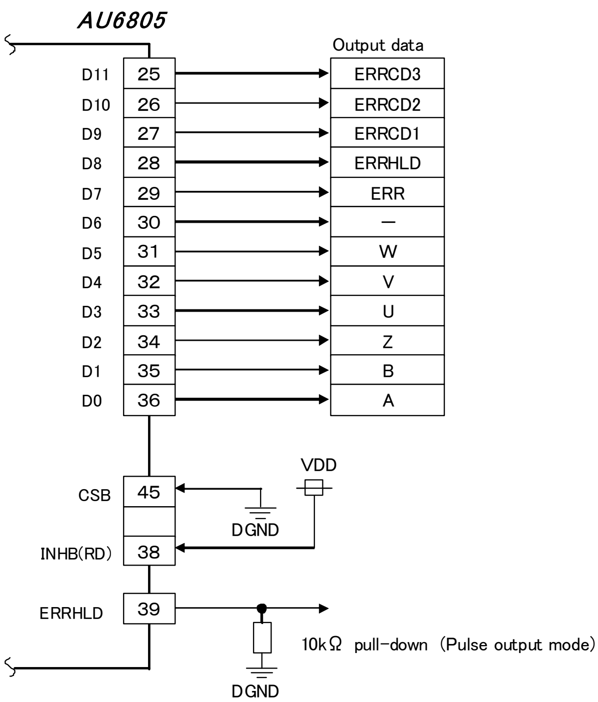


※Please refer chapter 10.9 for ϕ1～ϕ11、PRTY、CSB、INHB timing.

(Note) PRTY is an even parity output. The number of single digit will be even while data include parallel ϕ1～ϕ12 and PRTY.

■Usage of Pulse output mode

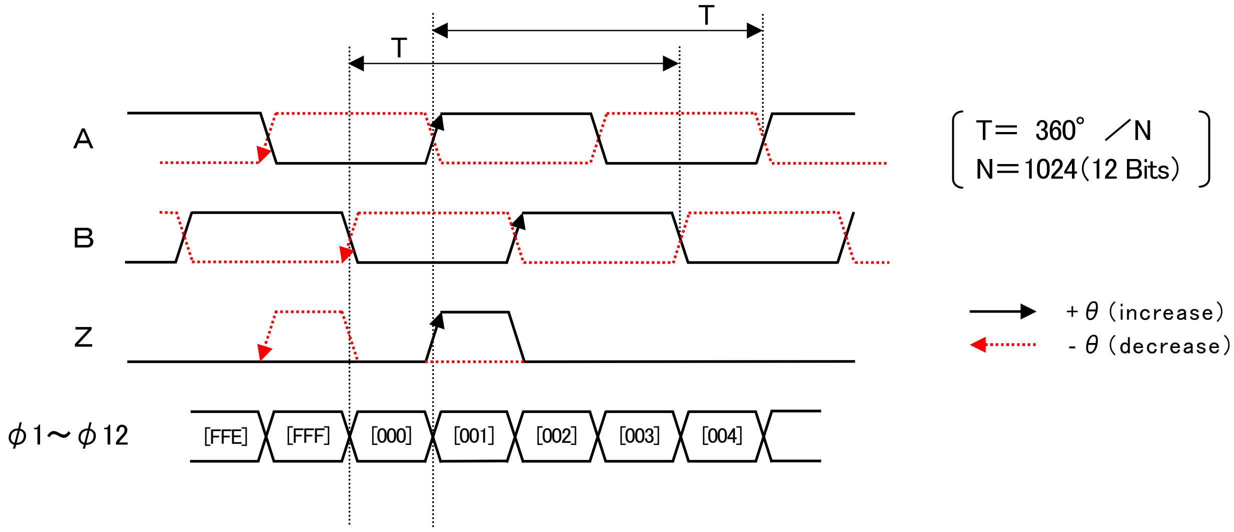
When it use in pulse output mode equivalent to an encoder, Set CSB="L" and INHB(RD)="H".

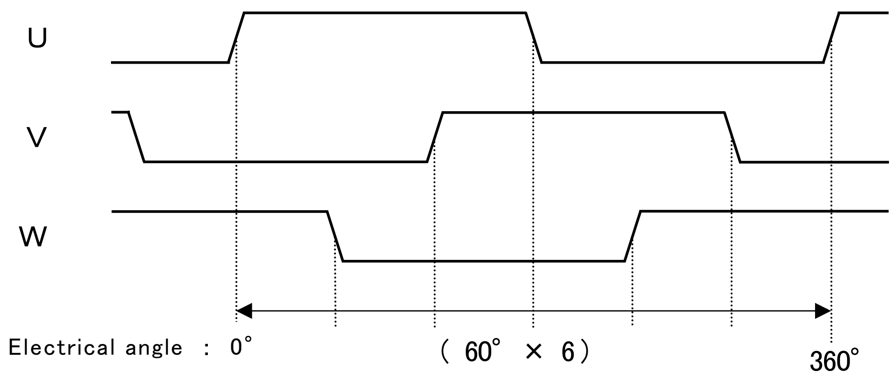


※A,B,Z pulse which come from D0~D2 pins are same signal with dedicated A,B,Z pin(42~44pin).

—Pulse output equivalent to an encoder—

The waveform of pulse output is shown below.





(Note) The pulses equivalent to an encorder may chatter at the edge of switching in some operating conditions. Note that the phase difference between A and B pulses and the width of pulses, etc. may be significantly disarranged. For purposes of preventing accumulation of angle error caused by chattering and electronic noise, etc., use a reversible counter on the signal processor side if using both A and B pulses.

(2) Serial output

This IC has a serial output data selection function that is defined by mode setting (Bit4, 3) of serial input setting register(refer 4.3.1(2)). Each serial output mode setting shows below output signals.

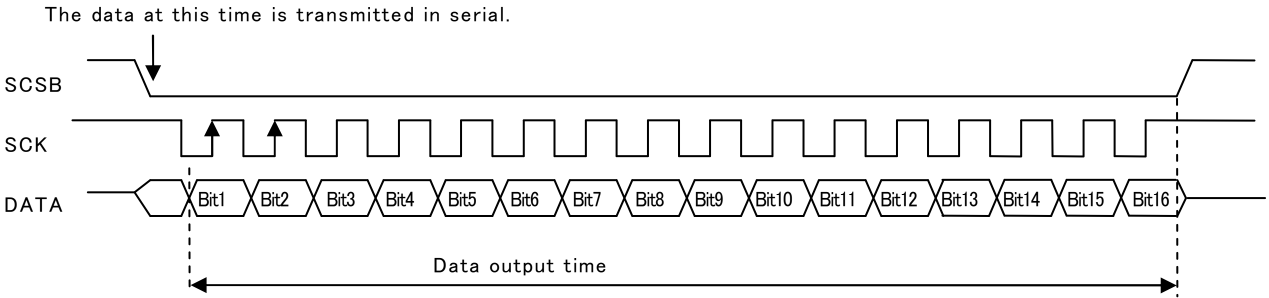
※When you set "Serial absolute output 16Bit mode"(Special mode), serial output becomes in absolute output 16bit mode regardless of setting resistor BIT No4,3 .

■Description of serial output signal

Serial output Mode setting [Bit 4,3]	"DATA" output Bit NO.															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Absolute output mode* setting [00]	LSB φ12	φ11	φ10	φ9	φ8	φ7	φ6	φ5	φ4	φ3	φ2	MSB φ1	PRTY	0	0	PRTY2
Pulse output mode setting [01]	Encorder equivalent Pulse						–	ERR	ERR HLD	ERR CD1	ERR CD2	ERR CD3	PRTY	1	0	PRTY2
	A	B	Z	U	V	W										
Serial callback setting [10]	Serial setting register contents												PRTY	0	1	PRTY2
	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit10	Bit11	Bit12				
BIST result setting [11]	Default setting		BIST CD1	BIST CD2	BIST CD3	BIST CD4	BIST 実行中	VMD	ERR HLD	ERR CD1	ERR CD2	ERR CD3	PRTY	1	1	PRTY2
	Bit 1	Bit 2														
Absolute out 16Bit mode [—](Special)	LSB φ16	φ15	φ14	φ13	φ12	φ11	φ10	φ9	φ8	φ7	φ6	φ5	φ4	φ3	φ2	MSB φ1

■Usage

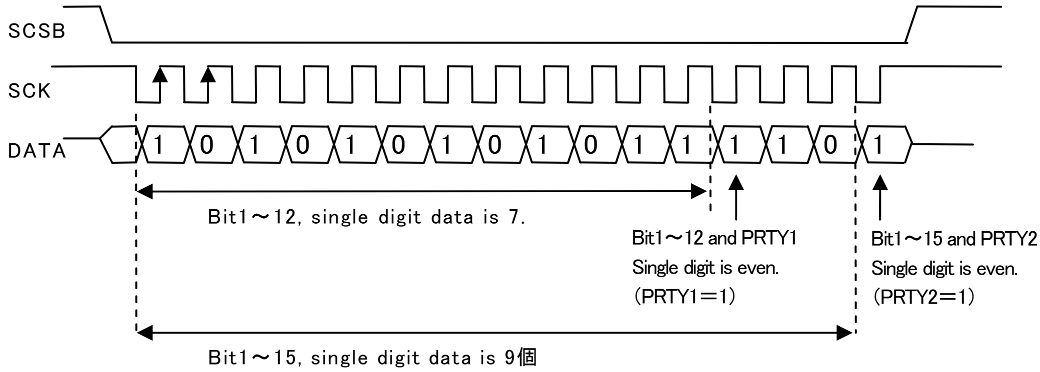
Serial output is controlled by SCSB/SCK pins. Serial data output from DATA pin with synchronized timing to SCK input at the active condition of SCSB input "L" lebel. DATA output switch at the falling edge of SCK, so please read output serial data at the rizing edge of SCK essentially.



※Please refer chapter 10.9 for each signal timing.

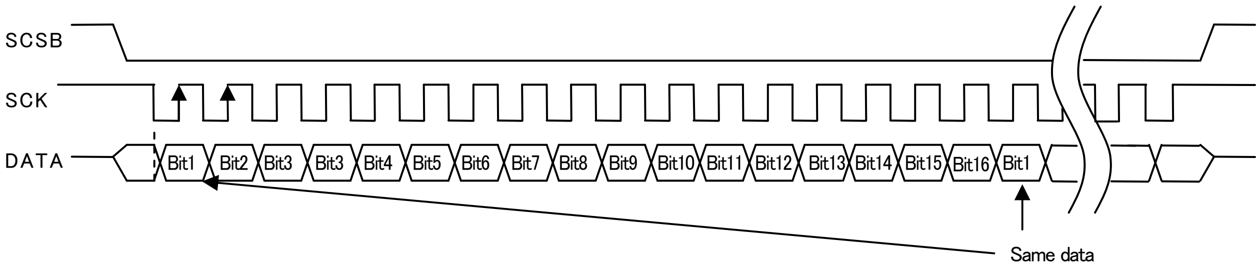
(Note) PRTY1/PRTY2 are even parity output. PRTY1 case, the number of single digit will be even while data include serial data bit Bit1～12 and PRTY1. PRTY2 case, it will be even while data include serial data bit Bit1～15 and PRTY2.

Example



Also while SCSB＝"L" fix and "SCK" clock keep to enter, serial output data will be repeated same data every 16 SCK clocks.

More than 17 SCK clocks



■Considerations for using the serial output

When using the serial output feature, please note the following points

① In serial output, required time to transmit all bits may generate some dead time in the control system. Especially it is possible to recognize the present position with some error in case of using the pulse output equivalent to an encoder.

② The effected signals by INHB are absolute output ϕ1～ϕ12, PRTY1, pulse output equivalent to encoder U, V, W, and ERR, ERRHLD, ERRCD1～3 、and serial output ϕ1～ϕ16 of absolute output 16Bit mode(special mode).

(3) A, B, Z independent pin output

A/B/Z pin (42~44pin) output the pulses equivalent to an encoder A/B/Z phase respectively. These independent output terminals are same signal with parallel output mode D0~D2. Please refer chapter 4.3.2(1) for signal timings, etc.

※A/B/Z independent outputs are outside the scope of the CSB input.

(4) Use verbose output

Each output signals described in 4.3.2(1)~(3) can use a combination of more than one signal.
Example the absolute value can be detected by using serial output and A/B/Z signals. Serial (absolute mode) data load after power on, and then absolute data can be caliculated by count up/down with A/B phase. It need total 6 I/O pins which mean 3 pins for serial and 3 pins for A/B/Z then you can reduce the I/O of the CPU. It can also be used for fault detection of digital output system by the combination of parallel output and serial output.
To suit individual applications and requirement, please utilize this verbose function.

※The pulses output (A,B,Z,U,V,W) equivalent to an encoder have a 1-bit hysteresis circuit to prevent chattering. Then there might have deviation against absolute angle data according to resolver rotation direction. The relationship between absolute angle data and encorder equivalent pulse refer to waveform of p39 figure.

4.3.3 Clock for Excitation

There is an clk selection function described in 4.3.1(1) default setting or 4.3.1(2) serial setting. An excitation clk can be generated from internal oscillator or external clock.

(1) Selection of internal oscillator

Using the IC's internal oscillator, then it does not need external clock. CLKIN:17pin (external clock) can be open.

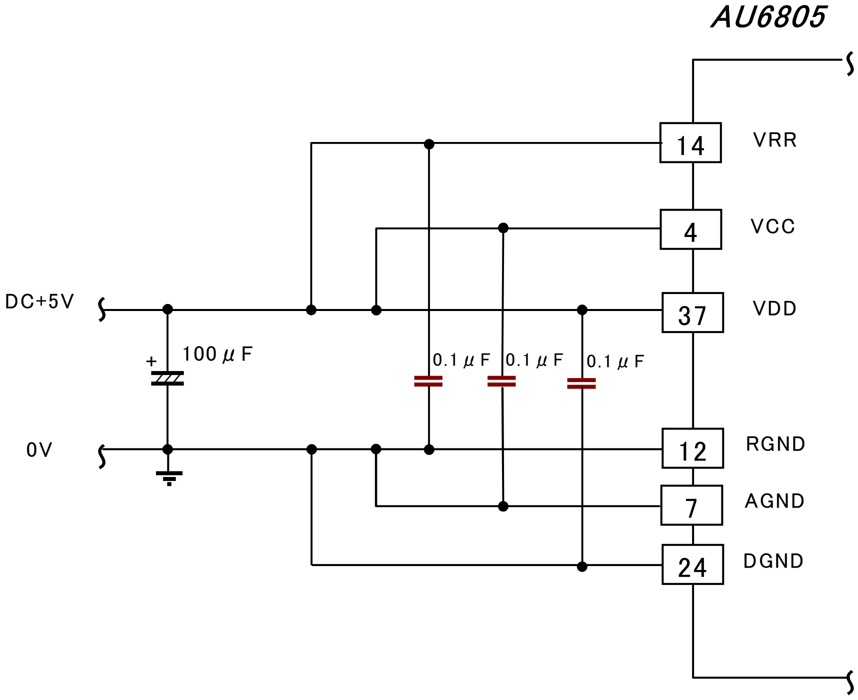
(2) Selection of external clock

This is useful to set the desired frequency of the excitation frequency. External clock should be input to CLKIN:17pin. This is CMOS-level pin.

Excitation frequenc = (External clock frequency)/1000

※ An external clock can be getting to be noise source. Then its board pattern must be as short as possible with guard GND pattern in order to make effective EMC measures.

4.4 Power Source



Power source is single supply +5V±5%. Analog power lines(VCC/AGND), digital power lines (VDD/DGND) and excitation power lines(VRR/RGND) must connect to each of the same one.

If you set separate power line for VCC-VDD−VRR or AGND-DGND−RGND, there must be no potential difference and power switching(On/Off) should be done simultaneously.

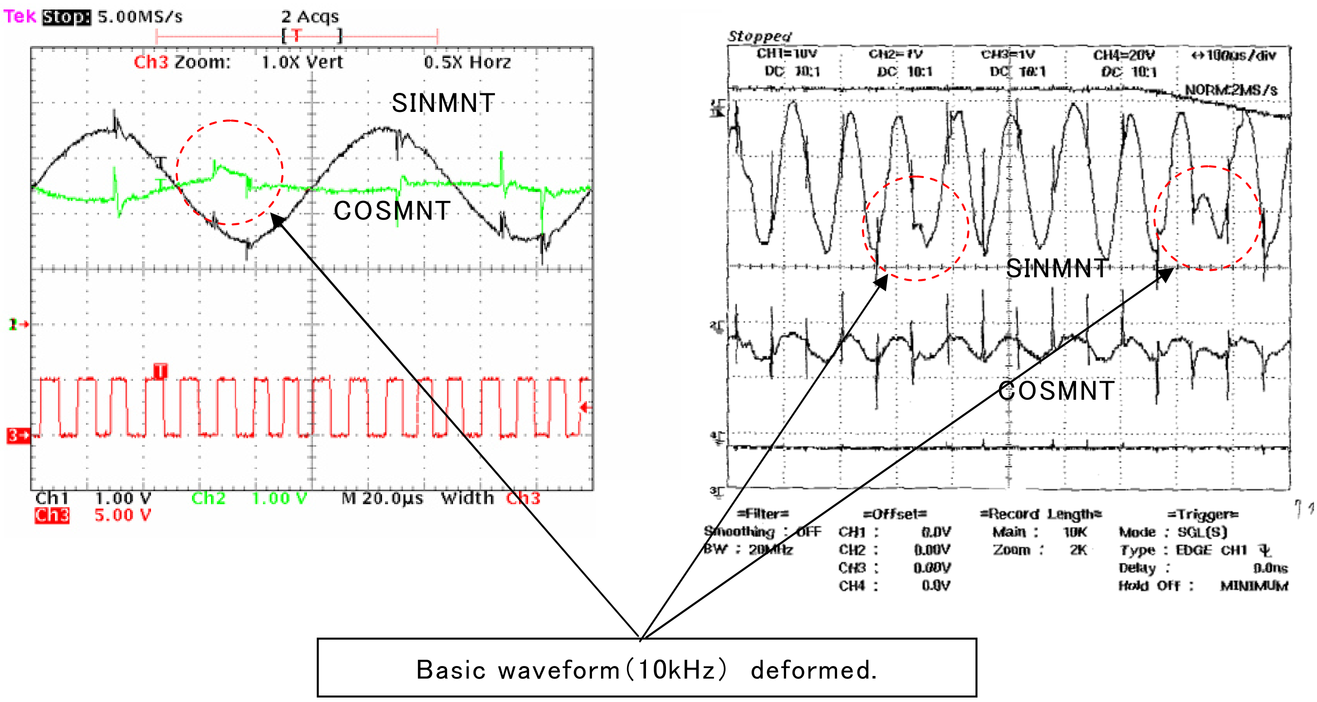
Above figure is example of power connection. Regarding 0.1uF capacitors, it should be located close to AU6805 device as much as possible.

4.5 Countermeasures for Noise

Below waveforms are measured actually. Countermeasure for noise must be done in accordance with the specification P34 contents.

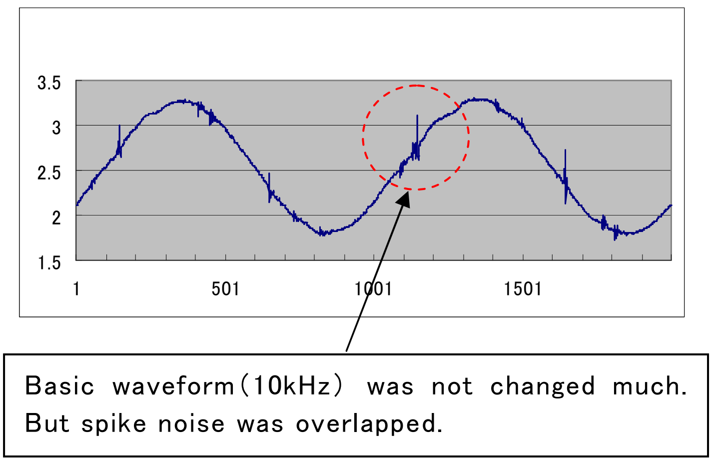
■Waveforms of magnetic noise

Magnetic noise happens when the leakage flux of the motor passes through the resolver. Its effect will be bigger turbulence of digital output, which will generate error.



■Waveforms of electrical noise

Electrical noise happens when the spike noise caused by PWM drive of the motor affects signal lines. Turbulence of digital output will not be so big but it will generate error depend on the size of noise.



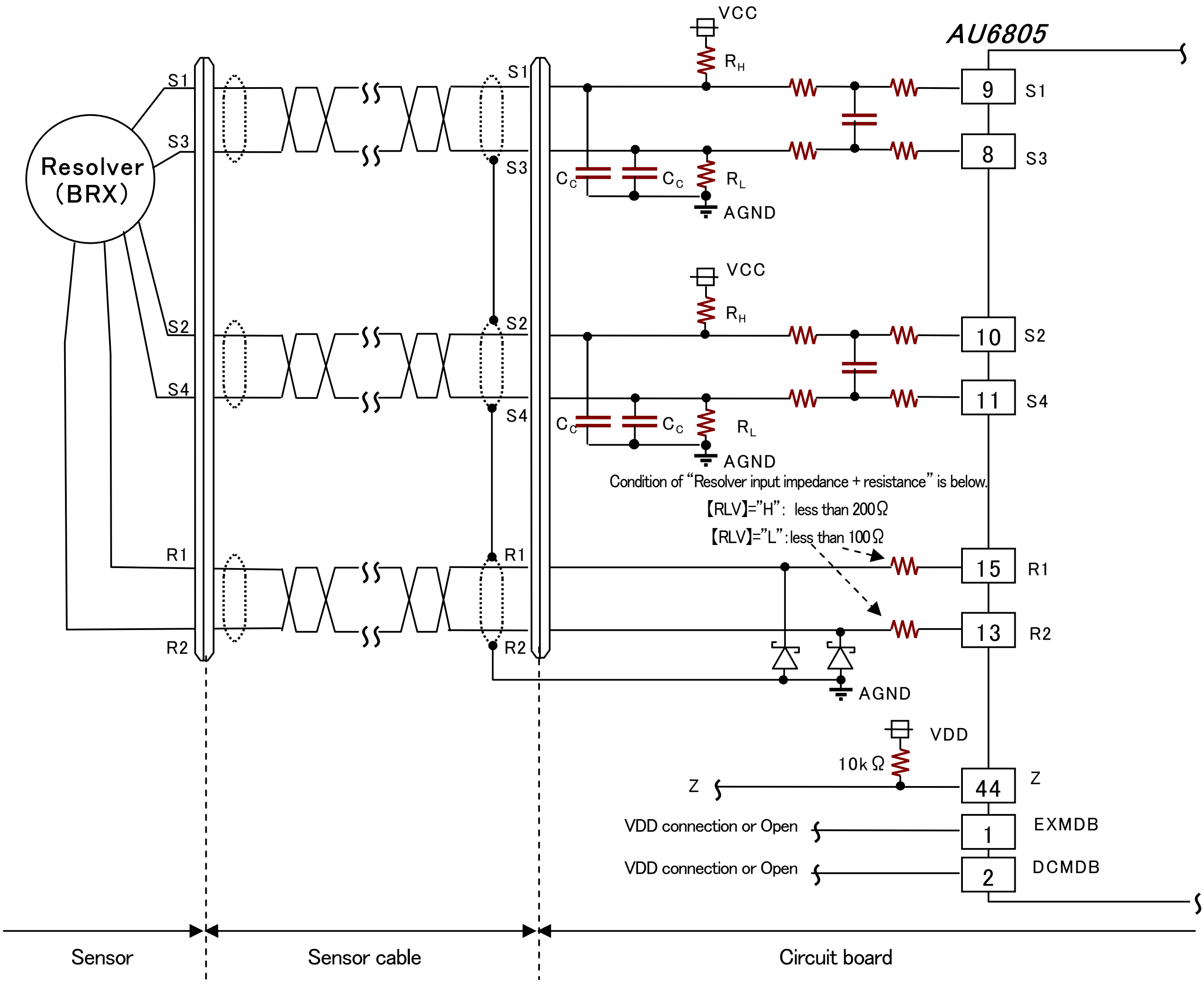
5. Connection

Caution !

Please take off the power during connection operation. After power off, take enough time, check the voltage value by tester, and please operate wiring and connecting.

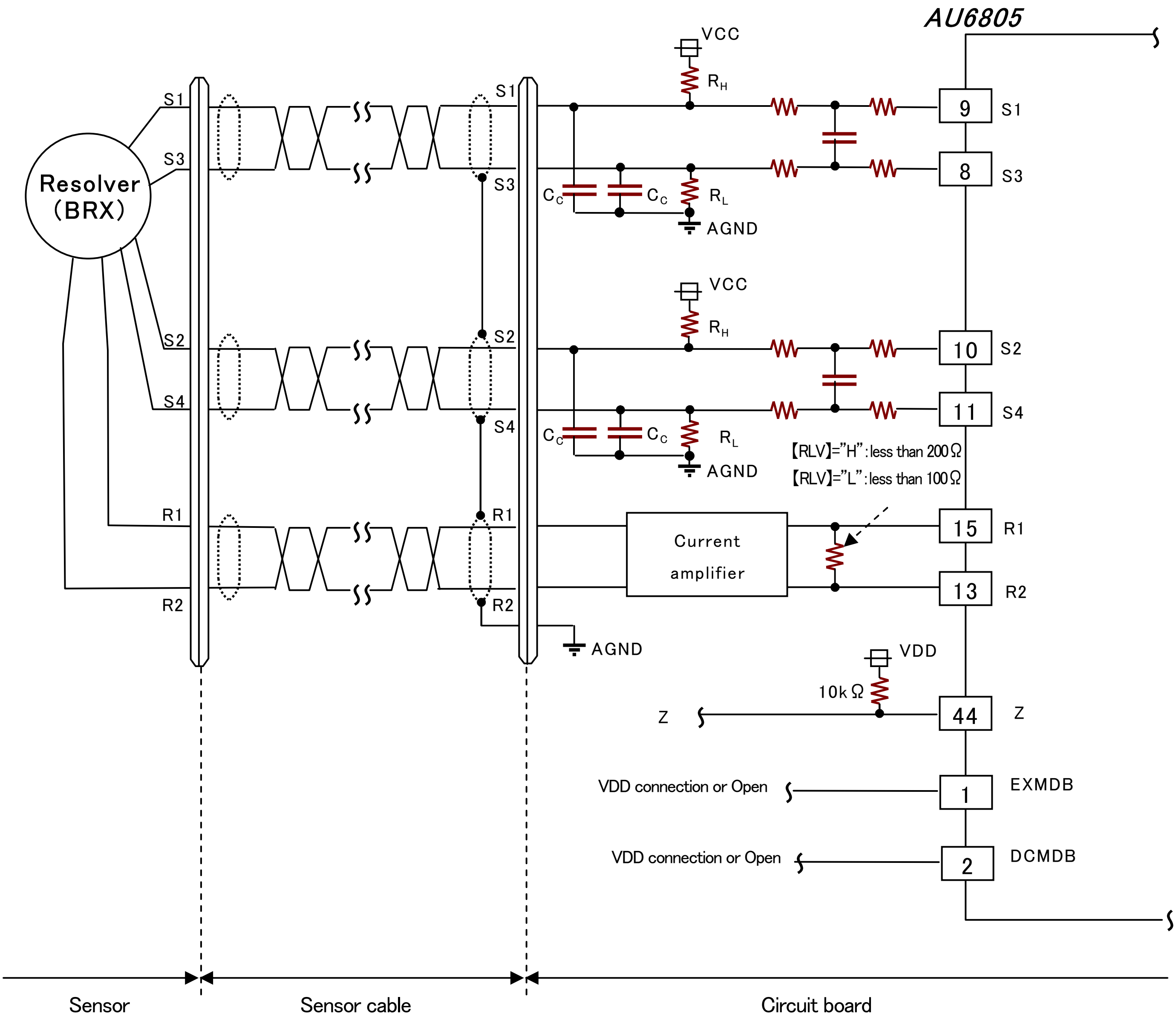
5.1 Example of Resolver Connection

■ Connenction and configuration example using direct excitation functions of this product.



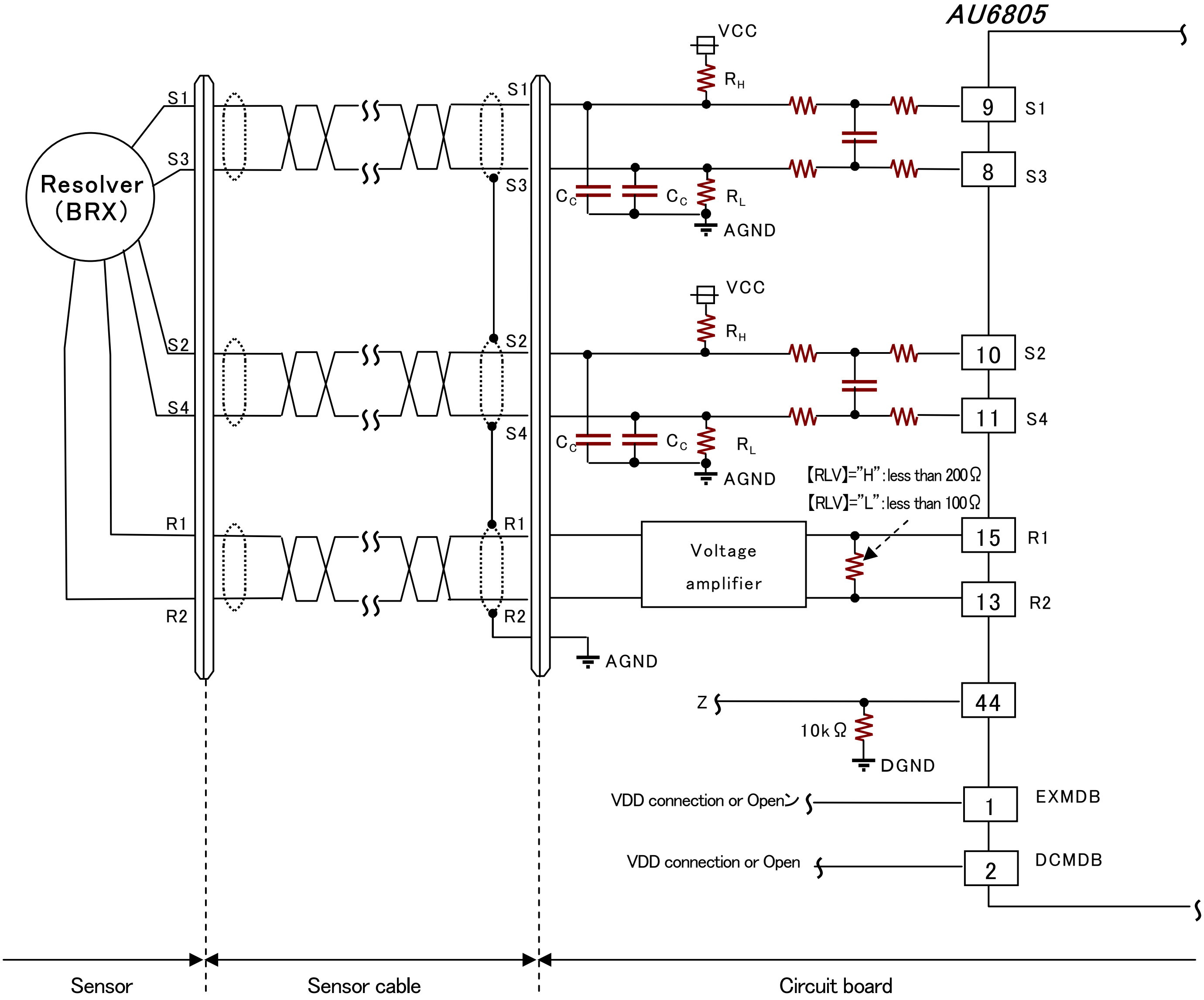
Resolver signals S1/S2/S3/S4 connects AU6805 terminals S1/S2/S3/S4 each via the resolver signal input circuit. And resolver signal R1/R2 connects AU6805 R1/R2. R1/R2 line will have series resistance and schottky barrier diode to measure noise inflow from resolver excitation line. When used in an environment with no surge they are not needed and will be no problem at function view point. EXMDB terminal connect VDD or OPEN(Internal pull-up), and R1/R2 set as current exciting output mode. At this direct excitation mode, normally use current excitation mode so please add 10kΩ pull-up resistance for Z terminal.

■Connenction and configuration example using external current amplifier to excite resolver



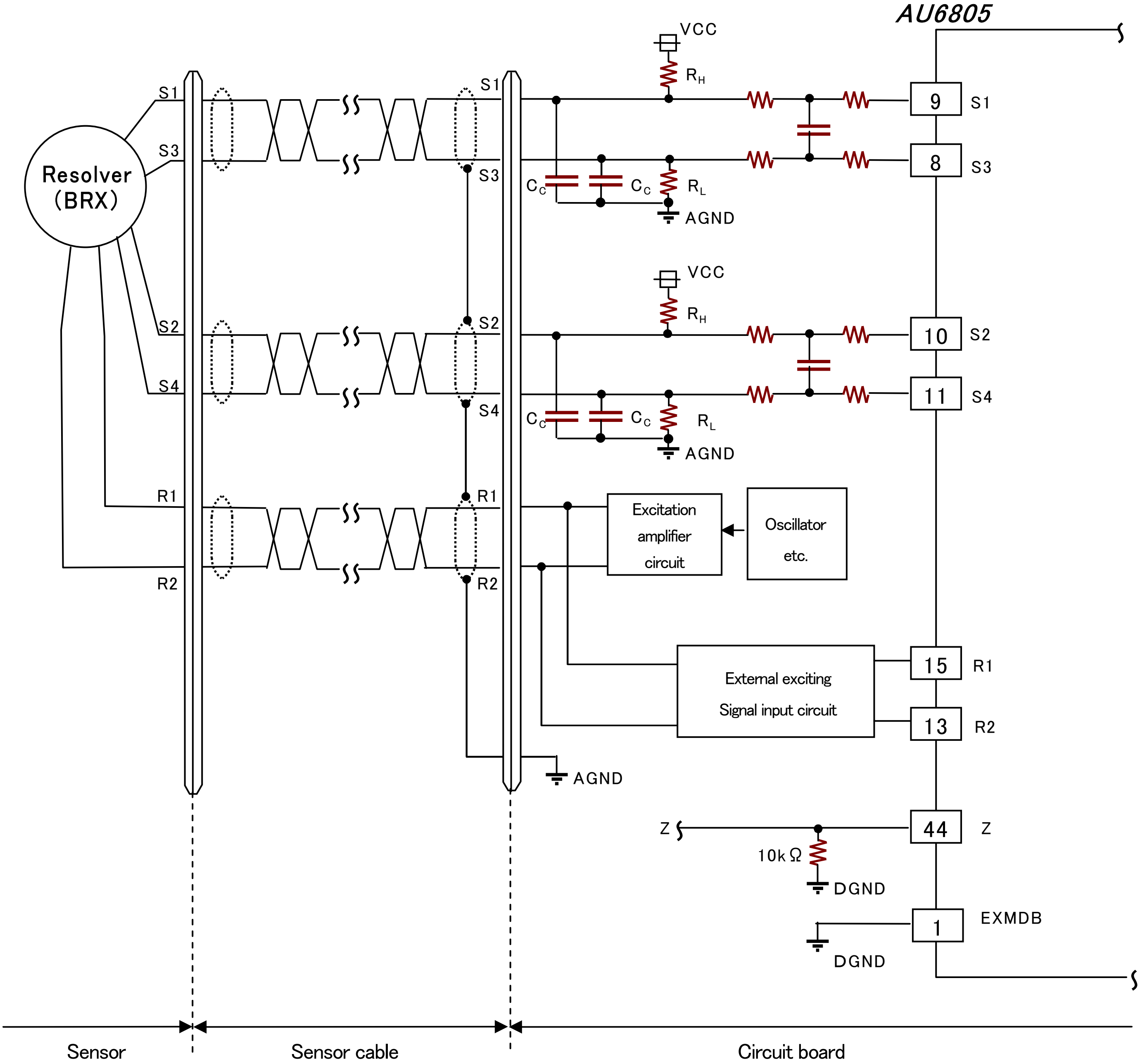
Resolver signals S1/S2/S3/S4 connects AU6805 terminals S1/S2/S3/S4 each via the resolver signal input circuit. EXMDB terminal connect VDD or OPEN (Internal pull-up), and R1/R2 set as current exciting output mode. The voltage generated across the resistor connected between the terminal of AU6805 R1 and R2 is getting to be source of current amplifier. The resolver R1/R2 signals connect to this current amplifier output terminal. When a resolver is excited by external current amplifier like this, normally use current excitation mode so please add 10kΩ pull-up resistance for Z terminal.

■Connenction and configuration example using external voltage amplifier to excite resolver



Resolver signals S1/S2/S3/S4 connects AU6805 terminals S1/S2/S3/S4 each via the resolver signal input circuit. EXMDB terminal connect VDD or OPEN (Internal pull-up), and R1/R2 set as current exciting output mode. The voltage generated across the resistor connected between the terminal of AU6805 R1 and R2 is getting to be source of voltage amplifier. The resolver R1/R2 signals connect to this voltage amplifier output terminal. When a resolver is excited by external voltage amplifier like this, normally use voltage excitation mode so please add 10kΩ pull-down resistance for Z terminal.

■Connection example: Used external oscillator as excitation source.



Resolver signals S1/S2/S3/S4 connects AU6805 terminals S1/S2/S3/S4 each via the resolver signal input circuit. EXMDB terminal connect GND, and R1/R2 set as external exciting signal input mode. Resolver exciting signal R1/R2 are connected to each corresponding AU6805 R1/R2 terminal through the external exciting signal input circuit.

※ （To an AU6802N1 experienced user）
AU6805 resolver signal input circuit has differenct with AU6802N1 case. Note that a connextion polarity of DC bias resistor(R_H、R_L) for break detection resolver signal is reversed.

5.2 Example of Power Connection

Refer the section 4.4

6. Check Point of Operation

> **Caution !**
>
> Before power-up, please make sure that the connections are no problem.

6.1 Check Point for Resolver Interface

6.1.1 Check Point of Excitation Signal

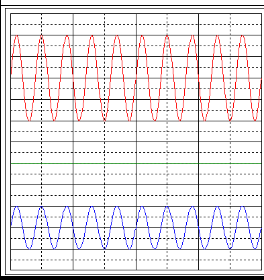
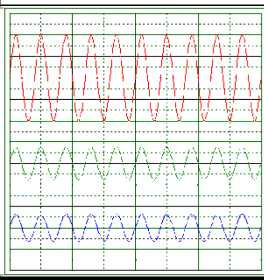
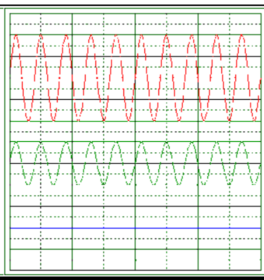
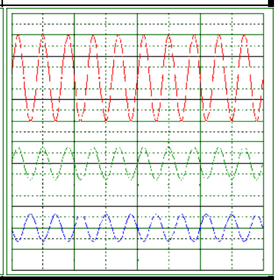
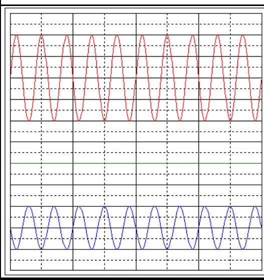
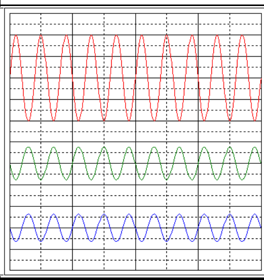
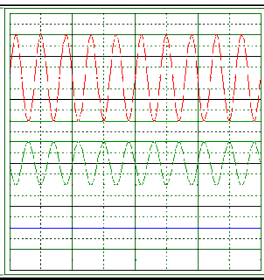
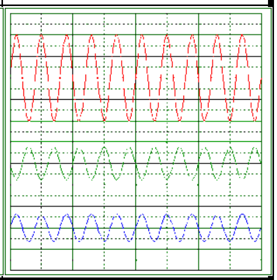
Check your resolver excitation signals (R1, R2) whether the resolver is excited with your designed amplitude or not. If signals are small or saturated situation, please check the suitability of the load and excitation circuit which connect to AU6805 excition output terminal again. If there are no signals, please check the connection to resolver and power supply status.

6.1.2 Check Point of Monitor Signal Amplitude

(1)Check point of amplitude change

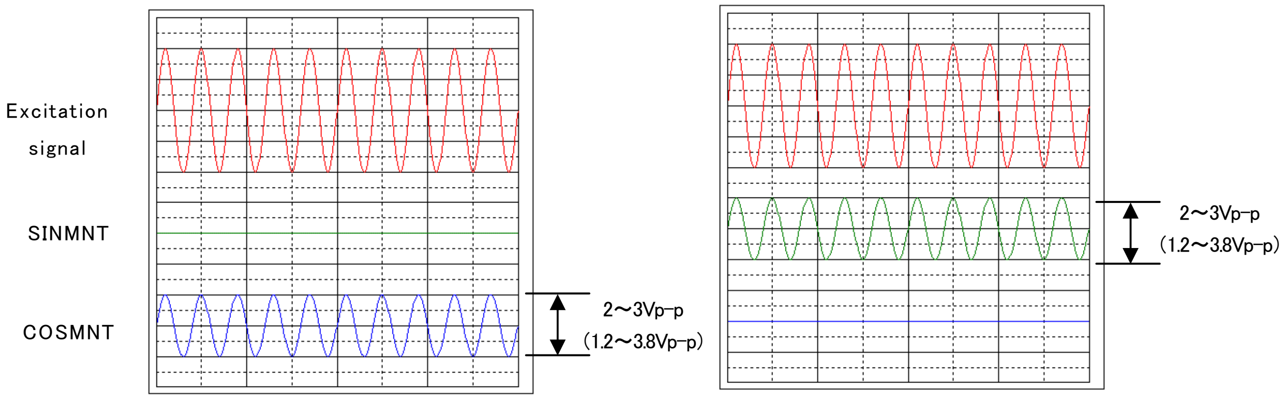
Observing the waveform of resolver exciting signals and monitor output （SINMNT、COSMNT), please check if the monitor output have a same frequency carrier of excitation signals. After then, rotate the resolver, please check that monitor signal amplitude is changing with corresponding resolver angle. If there is no signal or no amplitude change by rotation, please check the connection between resolver and AU6805.

■Waveform example of exciting signal and monitor signal with some fixed angle

Electrical angle	0°	45°	90°	135°
Excitation signal SINMNT COSMNT				
Electrical angle	180°	225°	270°	315°
Excitation angle SINMNT COSMNT				

(2) Check point of amplitude level

Rotating the resolver with observing a monitor signal waveform, please check the monitor signal maximum amplitude(at SINMNT Max location or COSMNT Max location). Maximum amplitude range of the most ideal resolver signal monitor output is 2～3Vp-p. While it is possible to make correct R/D conversion with 1.2～3.8Vp-p maximum amplitude output range which prevent detecting a resolver signal abnormality and Its range does not saturate the resolver monitor output signal. If signal amplitude is not appropriate range, please adjust your circuit constants of exciting amplifier and resolver signal input circuit.



6.1.3 Check Point of Phase Shift

(1) In case of resolver excitation using the excitation output of AU6805

In case of using AU6805 R1/R2 exciting output signal as direct excitation or excite signal source (P45/P46/P47 case), EXMDB terminal connect VDD or OPEN and R1/R2 set as current exciting output mode. And rotate the resolver with observing a exciting current output(R1-R2) of AU6803 (AU6804) and a monitor output voltage waveform. Then please check the phase difference between a excitation waveform component of R1-R2 current output and a excitation waveform component of the output voltage monitor while both measurement signals are same phase. Measuring phase difference must be inside below range of setting excitation-mode. When phase difference is outside the acceptable range, please set an appropriate excitation-mode to make phase difference inside the acceptable range.

Setting of excitation mode	Phase shift acceptable range
Current excitation mode (VMD="0")	+90° ±45°
Voltage excitation mode(VMD="1")	0° ±45°

※ please note that above phase difference criteria based on AU6805 current output phase(R1-R2). It does not based on Voltage output phase(R1-R2).

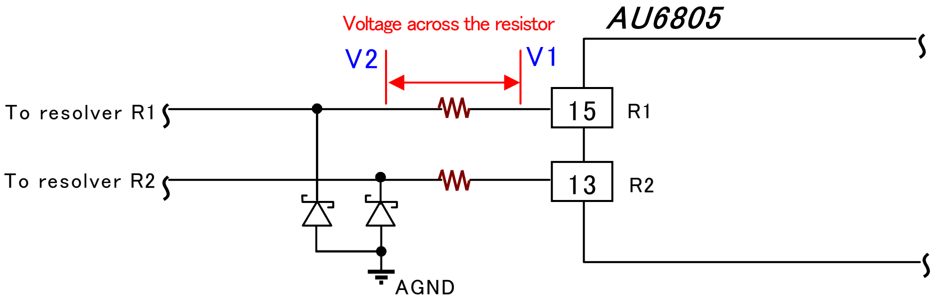
■How to check the current phase of excitation output

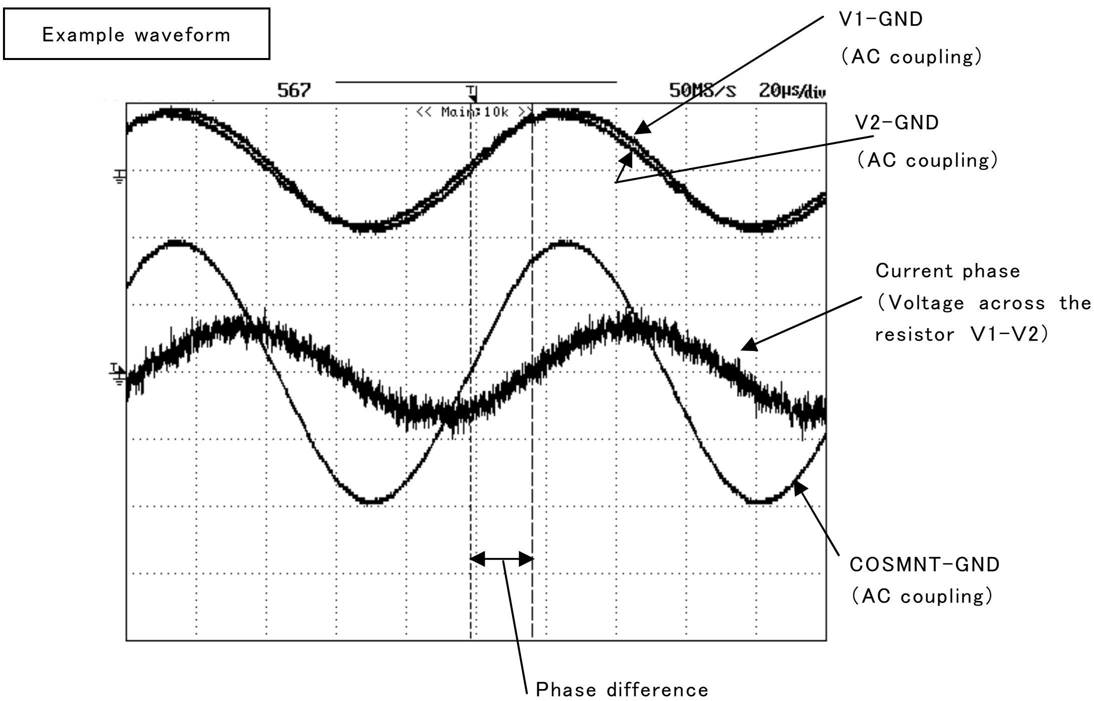
When you check the current phase of AU6803(AU6804) excitation output(R1-R2) by oscilloscope, please prepare current probe. Otherwise you can confirm it by the following methods which fit for each excitation mode.

Caution !	If the R1 or R2 terminal is short-circuited to GND or the power line (VRR/VCC/VDD etc), It may cause damage. When the waveform between R1 and R2 need to be checked, it can get by the difference of each waveform. Never connect probe-GND directly to the R1 or R2 terminal.

—In case of using direct excitation function(Current mode) of this product.—

If R1/R2 lines have series resistance and schottky barrier diode to measure noise inflow from resolver excitation line, you can measure the voltage phase across the resistor inserted in series as the desired current phase. Then you can see the current phase with measuring the voltage waveform across the resistor in series either.

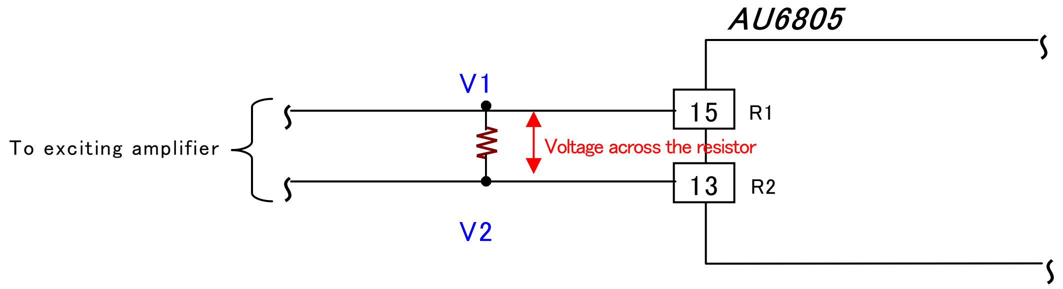




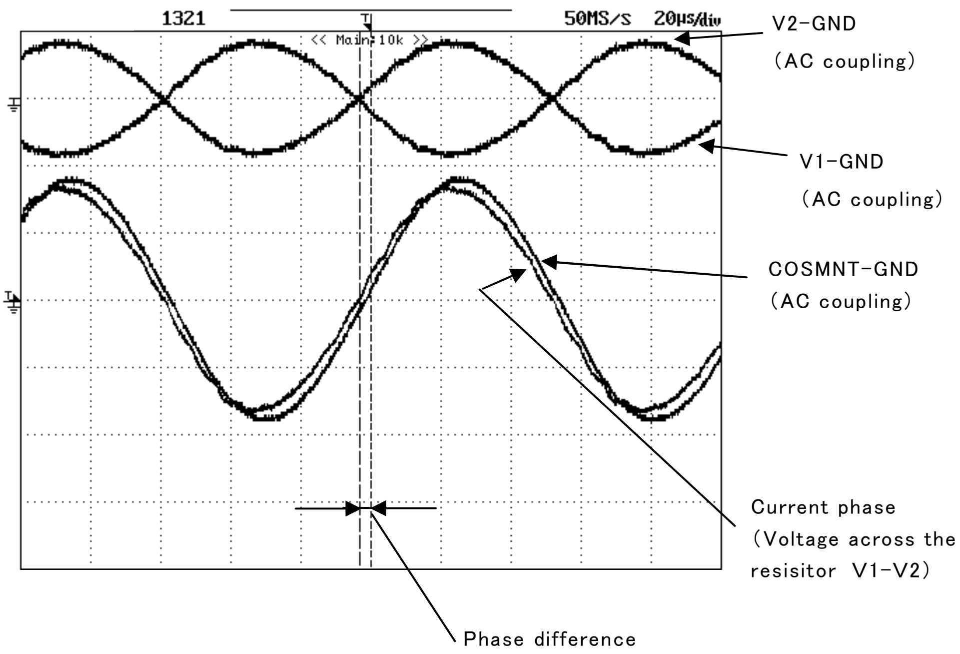
※The above example is for the phase advance case of voltage monitor signal.

—In case of using external amplifier to excite resolver—

An external excitation amplifier (either voltage-type and current-type) need input as voltage source which is converted from exciting current output of AU6805 by inserting a resistor between R1 and R2 like below. Then this voltage phase of across the inserting resistor is getting to be same as the desired current phase. So you can get the current phase with measuring the voltage waveform across the inserting resistor.

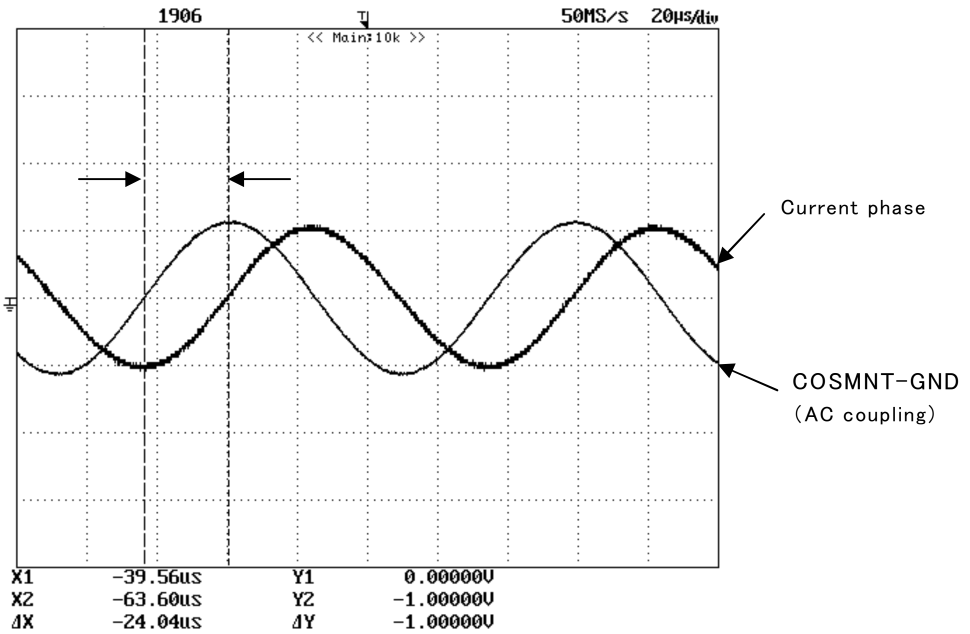


Example waveform



※The above example is for the phase delay case of voltage monitor signal.

■How to convert an angle of phase shift



Phase shift[°]=360[°]×(Time shift[μs]／Exciting frequency period[μs])

Above case:Exciting frequency=10kHz → Period=100μ(=1/10kHz)
Time shift=24μs
Phase shift=86.4° (=360×24／100)

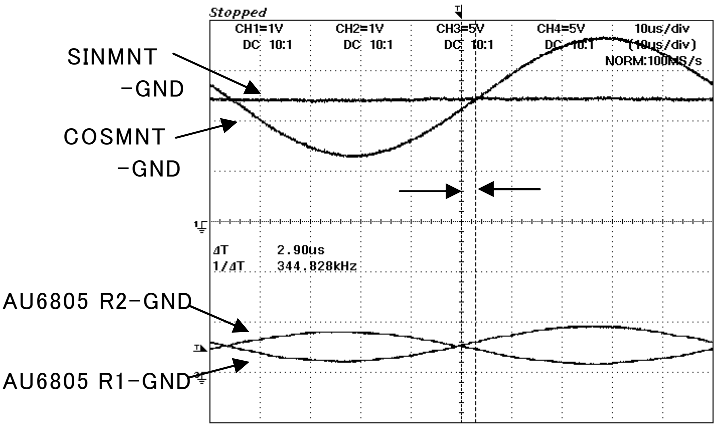
(2)In case of resolver excitation using the external source(Oscillator etc.)

In case of using AU6805 R1/R2 exciting output signal using external signal source(P48 case), EXMDB terminal connect to GND. Rotating the resolver with observing a momitor signal and differential signal(Voltage of R1−R2) of external input. Then please check the phase difference between a excitation waveform component of R1−R2 voltage and a excitation waveform component of the output voltage monitor while both measurement signals are same phase. The phase difference should be within ±45° .

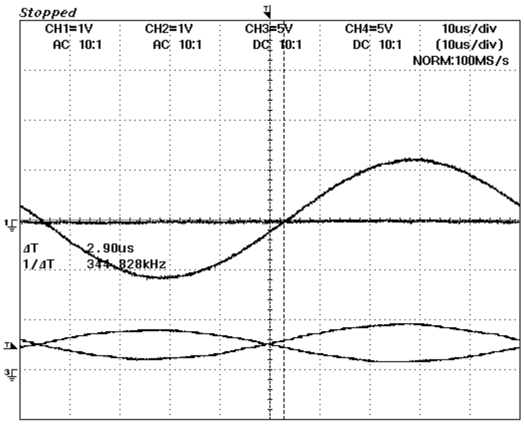
※ In above case, the phase difference criteria based on the voltage phase of AU6805 exciting terminal(R1−R2).
This is different with EXMDB="H" setting case.

■How to convert an angle of phase shift

Monitor out signal DC coupling example



Monitor out signal AC coupling example



Phase shift[度]＝360[度]×(Time shift[μs]／Exciting frequency period[μs]

Above example:Exciting frequency＝10KHz → Period＝100μ(＝1/10KHz)
Time shift＝2.9μs
Phase shift＝10.4° (＝360×2.9／100)

6.2 Check Point for Digital Output

6.2.1 Check Point of Output Angle

Please check that the each digital output show your required format which you set and angle output data is changing with resolver rotation. If angle output is not change while resolver rotation or output format is different with your setting, please check a polarity of each digital input terminal. Also if output angle data does not match with actual angle or output data is not stable, refer section 6.1 and please check if there is no problem for resolver related connections.

6.2.2 Check point of abnormality Detection

"ERR" output assumed L-level. And "ERRHLD" output during "ERRHLD" output H-level also assumed L-level. Please check that both signal (ERR and ERRHLD) shows L-level. If this device detects some error condition, "ERR" output or "ERRHLD" output will be H-level. Then you may refer section 9.1 and please isolate the true cause of the error and remove it.

7. Built In Self Test(BIST)Function

AU6805 has a built-in self test function and you can determine the validity of operation by excuting this BIST function sequence. The details of the diagnosis are described below.

・BIST of R/D conversion: Self-diagnosis function of R/D(angle) conversion. It is self tested by means of the electrical angles of 0, 45 or 270 degrees set as the resolver signal input.

・BIST of failure detection: Self-diagnosis function of failure detection. Set the simulated abnormal conditions and possible to determine the validity of the failure detection operation. It include below.

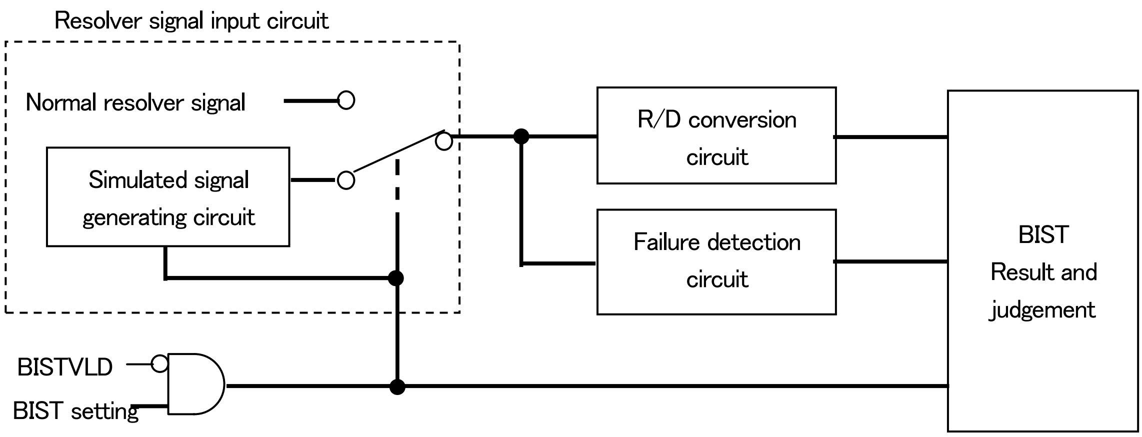
■BIST of signal abnormal detection: "Resolver signal abnormality" detect BIST.
■BIST of signal disconnection edtectoin: "Resolver signal disconnection" detect BIST.
■BIST of conversion abnormality: "R/D conversion abnormality" detect BIST

In this section, we explain the operation, how to excute, and diagnostic results of BIST.

7.1 Run-Time Behavor of BIST

BIST functions test to determine the validity of the failure detection function by generating a required simulated signal inside IC and monitoring the output signal. While each BIST is executing, device operations which is R/D conversion and failure detection are switched to work on simulated signal base. Then please note that normal operation using external resolver input signal becomes invalid while excuting BIST.

■BIST circuit schematic configuration

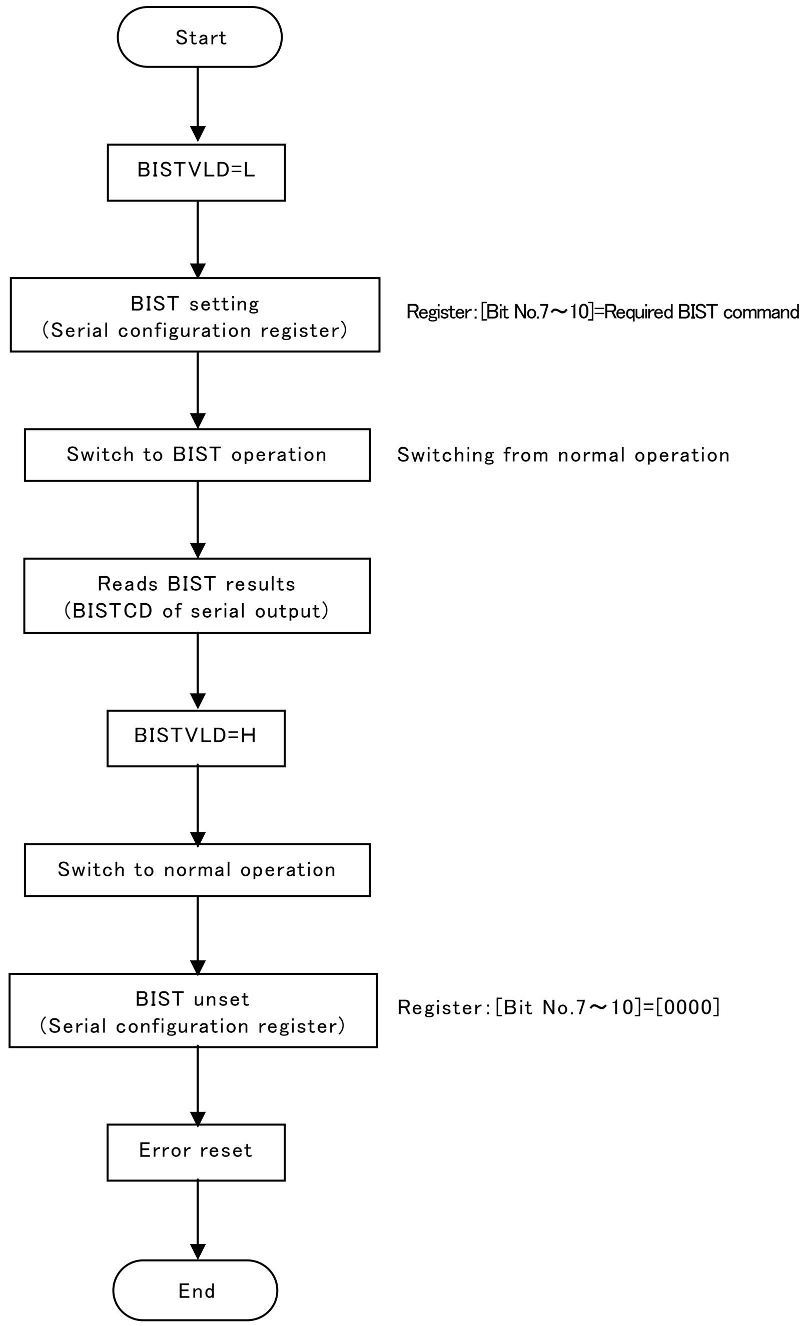


7.2 Execution Method of BIST

BIST function is active when "BISTVLD" input is "Low". And BIST will be excuted while configuration registers (Bit No 7˜10) has been set. The result can read by serial output BIST code (BISTCD1˜BISTCD4) when BIST is excuting. The following shows the basic execution flow.

■ BIST execution flow.

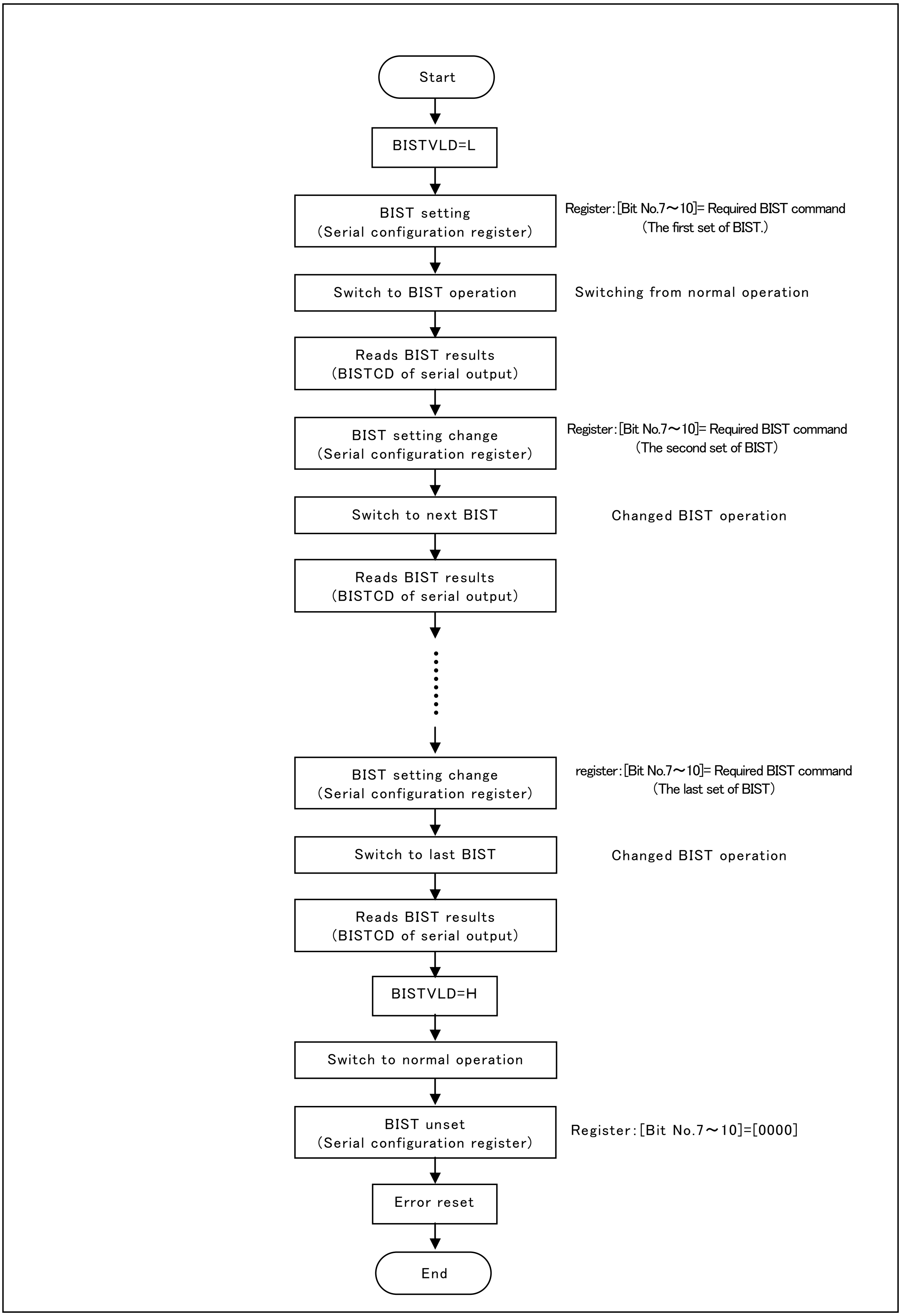
—If you run only a specific set BIST.—



※ The order is not issue for "BISTVLD=L switching" and "BIST setting". The reverse case, switching to BIST operation is getting valid by "BISTVLD=L switching".

※ The order is not issue for "BISTVLD=H switching" and "BIST unset". The reverse case, switching to normal operation is getting valid by "BIST unset".

—If you run multiple consecutive BIST configurations—



■Considerations for BIST execution

When you perform BIST, please note the following points.

① The error reset should be performed after BIST operation is completed.

② Please set more than 10ms latency and set resolver rotation speed less than 120,000min^{-1} to excute error reset after switching to the normal operation mode from BIST mode.

③ The BIST result read timing of "normal mode to BIST start → reading BIST result" or "BIST operation to BIST setting change → reading BIST result" refer to the following.

■BIST judgement time

Judgement item	Judgement time	Remarks
Angle conversion BIST	10ms max	Waiting time to stable BIST judgement result.
Resolver signal abnormality BIST	0.5ms max.	
Resolver signal disconnection BIST	1ms max.	
R/D conversion abnormality BIST	10ms max.	

7.3 Result of BIST

Each BIST result indicate their specific code of BISTCD1~4 which is assigned as Bit3~6 of serial output mode [11](Result of BIST). The diagnosis result that is falling edge timing of SCSB output as serial data.

■Description of BIST results

BIST CD4	BIST CD3	BIST CD2	BIST CD1	Description of BIST results	Remarks
0	0	0	0	(Default value)	Except on BIST
0	0	0	1	—	
0	0	1	0	—	
0	0	1	1	—	
0	1	0	0	—	
0	1	0	1	Match BIST ordered angle(0°)	Match range:within±1.4°
0	1	1	0	Match BIST ordered angle(45°)	Match range:within±1.4°
0	1	1	1	Match BIST ordered angle(270°)	Match range:within±1.4°
1	0	0	0	—	
1	0	0	1	Resolver signal abnormality BIST detected	
1	0	1	0	Resolver signal disconnection(COS)detected	
1	0	1	1	Resolver signal disconnection(SIN)detected	
1	1	0	0	R/D conversion abnormality detected	
1	1	0	1	—	
1	1	1	0	—	
1	1	1	1	BIST abnormality or special mode operation	

8. Function of Fault Detection

AU6805 has built-in test function of fault detection. These error conditions output at the "ERR" or "ERRHLD" terminal and error code which describe error contents output from the ERRCD1~3 by output setting. The 4 kind of contents of detection are shown below.

- Resolver signal abnormality
- Resolver signal disconection(DC-bias method)
- R/D conversion abnormality(Control excessive deviation)
- Abnormal high temperature inside IC

In this chapter, describe each detection method and typical fault detection pattern and also describe corresponding error code, their priorities, and error reset method.

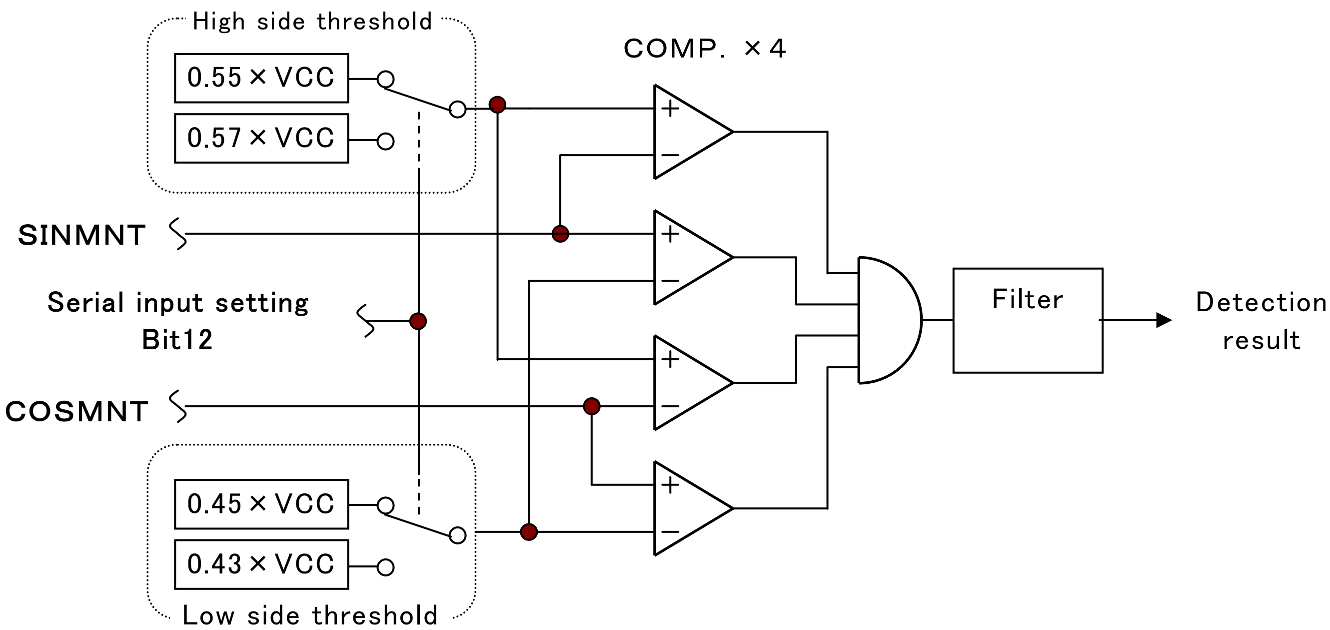
This built-in test function is independent from R/D conversion function and does not restrict any output of R/D conversion IC as a result of this failure.

8.1 Abnormal Resolver Signal

8.1.1 Concept Detection

This concept is to detect smaller monitor output amplitude level then it defines as abnormal resolver signal. Breaking/down of exciting line can not excite resolver, then a resolver output signal will diappear and abnormal resolver signal can be detect. In case of the state of abnormal detection condition, fail condition like "short condition between the signal line(S1-S3, S2-S4)" or "Rare short of resolver winding" can be detect with this method.

8.1.2 Circuit Configuration



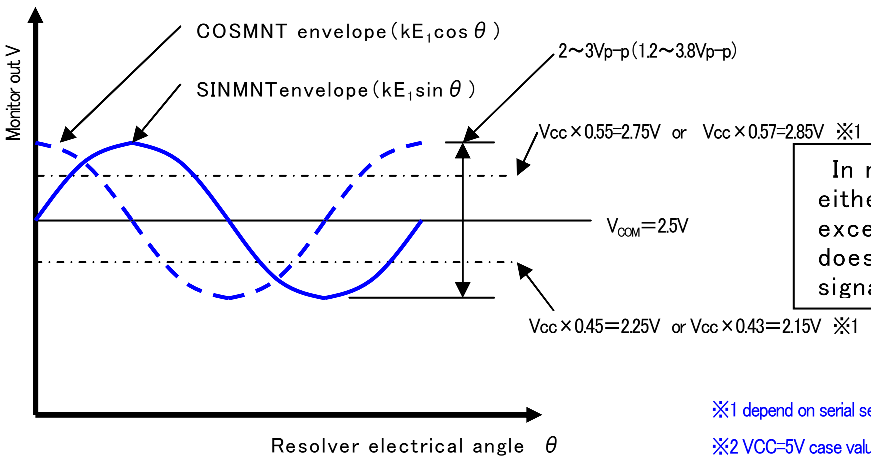
8.1.3 Detection Principle

This detection principle is a comparison between monitor output and threshold voltage. This method detect situation that the both monitor voltage magnitude of SINMNT and COSMNT are above low-side threshold and below high-side threshold. This means that both monitor signal amplitude is under 0.1×VCC(Vp-p) in case of serial input setting BIT12="L", or amplitude is under 0.14×VCC(Vp-p) in case of serial input setting BIT12="H". These condition can be detect as abnormal.

※Example of VCC-5V case, serial input setting Bit12=L" case, abnormal detection condition is that the both monitor amplitude is under 0.5Vp-p.

8.1.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal

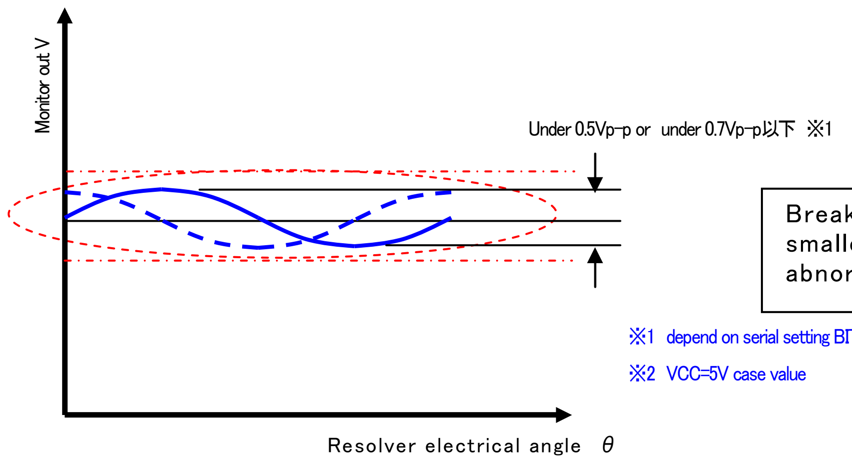


In normal monitor signal case, either SINMNT or COSMNT exceed a threshold value. Then it does not detect abnormal resolver signal.

※1 depend on serial setting BIT12

※2 VCC=5V case value

(2) Detection pattern① (Monitor amplitude is under threshold)

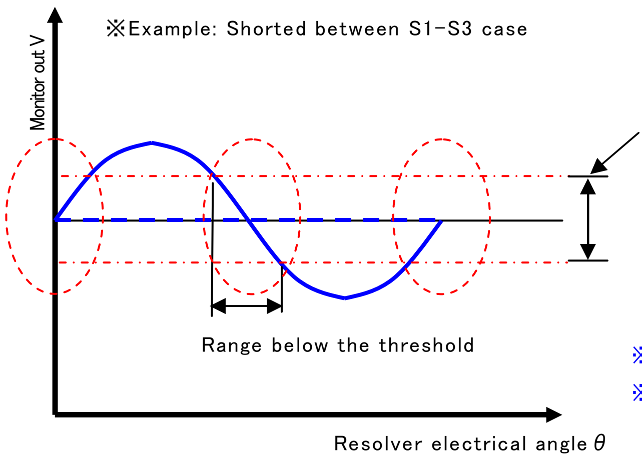


Breaking/down of exciting circuit or smaller monitor output will detect as abnormal signal in full angular range.

※1 depend on serial setting BIT12

※2 VCC=5V case value

(3) Detection pattern② (Shorted between S1-S3 or S2-S4)



Under 0.5Vp-p or under .07Vp-p ※1

In case of short between S1-S3 or S2-S4, when normal monitor amplitude go under the threshold value, error can detect in such angle range.

※1 depend on serial setting BIT12

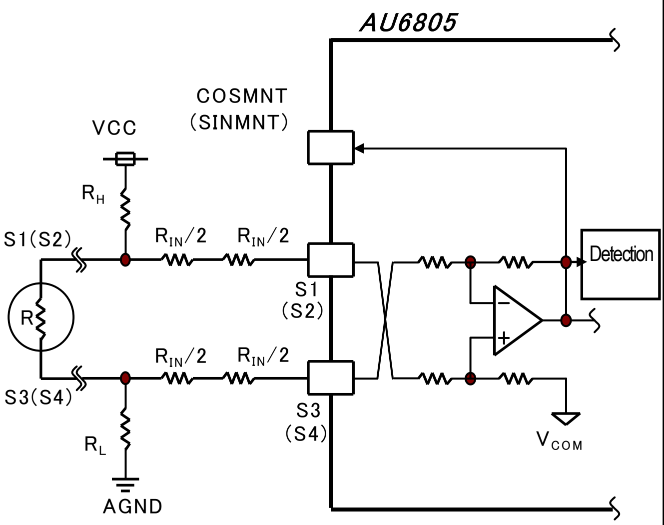
※2 VCC=5V case value

8.2 Disconnection of Resolver Signal Line (DC-bias method)

8.2.1 Concept Detection

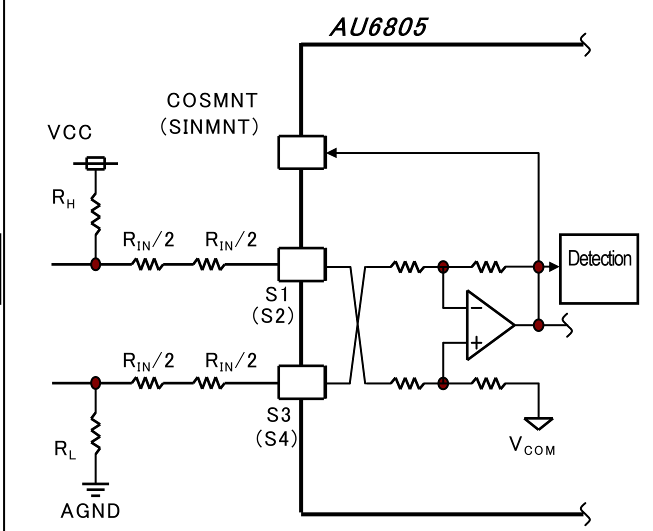
In the resolver signal input circuit, applying the external DC bias circuit(refer 4.2.2) will detect DC level shift. When the resolver signal line is disconnected, corresponding monitor output will shows DC level shift to VCC-side against the reference V_{COM} voltage. This detection concept is to detect a DC level shift of internal resolver signal.

【DC view:Normal-resolver signal input circuit】



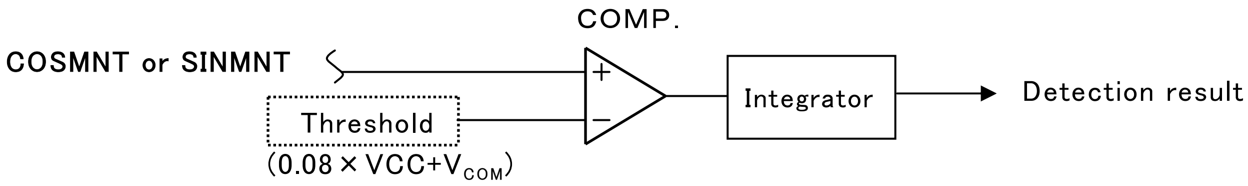
Resolver DC resistance【R】 ≪ DC bias resistance【R_H or R_L】 Then resolver terminal S1/S3(or S2/S4) are same potential. So monitor output(Differential amplifier circuit output) is same as reference voltage(V_{COM}) in DC view point.

【DC view: resolver signal disconnection case 】



When signal line is disconnected, "VCC-GND" will be entered to differential amplifier input. Then monitor output will be shifted to VCC-side against the reference voltage(V_{COM}).

8.2.2 Circuit Configuration

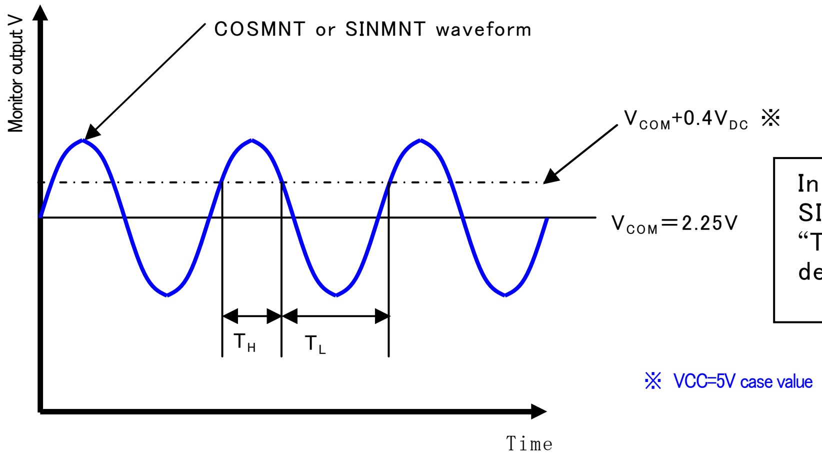


8.2.3 Detection Principle

The principle is comparison between internal resolver signal voltage and threshold. If the time which counts below the threshold is longer than the time(T_L) which exceeds the threshold, it is detected as fault situation.

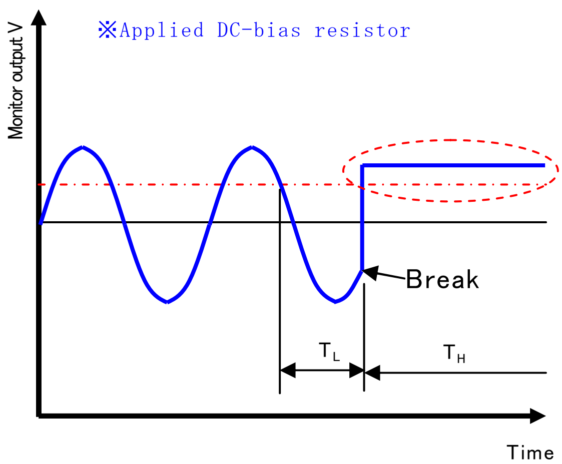
8.2.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal



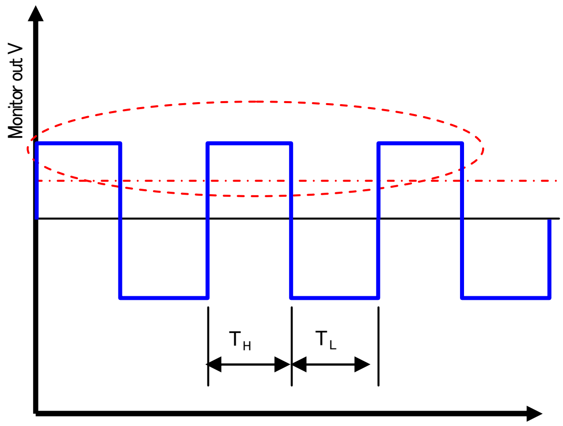
In normal monitor signal case, both SINMNT and COSMNT shows "T_H<T_L" condition then it does not detect as fault.

(2) Detection pattern③ (Disconnection between S1-S3 or S2-S4)



In case of breaking signal line, the monitor output DC level will exceed threshold value due to DC bias resistance and this "T_H>T_L" situation can detect as fault.

(3) Detection pattern④ (Rectangle monitor output waveform)



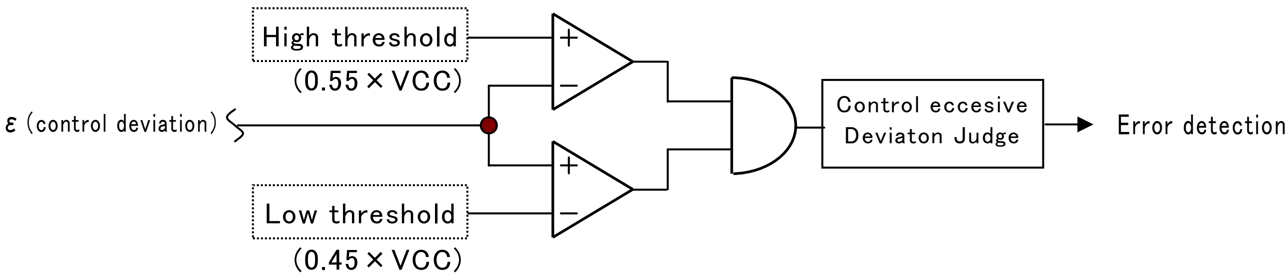
When the monitor output is in a rectangular wave to be saturated, it will be "T_H=T_L" condition then it might be detected as fault situation due to boundary conditions for the determination.

8.3 Abnormal R/D conversion (Excessive control deviation)

8.3.1 Concept Detection

This product adopted digital tracking method (Refer section 1.3 or 11.1) as R/D conversion system, and this method is one of the negative feedback control of closed-loop configuration. In such a system, normally control deviation (ε) should be "0". This idea of the detection is that the excessive control deviation assumed to mean out of control and that situation is detected as abnormal.

8.3.2 Circuit Configuration



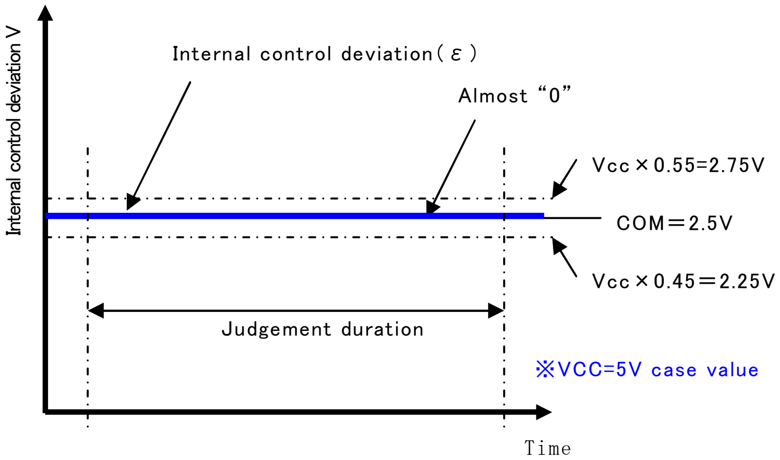
8.3.3 Detection Principle

This detection principle is to compare the internal control deviation(*1) and the threshold value. If there are situation that the absolute value of internal control deviation is less than low threshold or bigger than high threshold, and if this situation is over 50% of test duration(*2), then it is detected as fault.

※1 A internal control deviation signal can not be verified.
※2 Judgement duration is about 5.9ms.

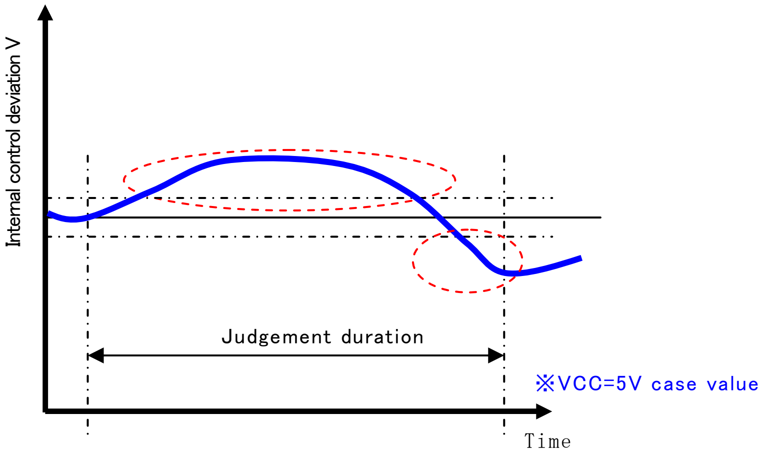
8.3.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal



In the state that it bave been successfully R/D converted, control deviation is almost "0". Then it is not detected as fault.

(2) Detection pattern⑤ (Excessive control deviation)



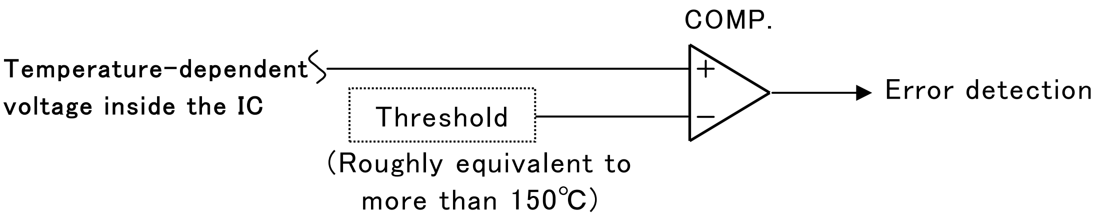
There is an abnormal R/D conversion situation (control deviation exceed the threshold), and if such situationis over 50% of judgement duration, it is detected as fault.

8.4 Abnormal High Temperature inside IC

8.4.1 Concept Detection

In this detection concept, a state which the IC junction temperature exceed 150℃ is defined as a state leading to product failure, then it is detected as fault. The product which is detected as this abnormal high temperature might be damaged their circuit by heat even back to the normal state. So please do not use such products.

8.4.2 Circuit Configuration



8.4.3 Detection Principle

The principle is to make comparison between the generating voltage which characteristic depend on the temperature at the internal and threshold voltage which equivalent to more than 150℃. If it exceeds the threshold temperature it is detected as fault.

8.4.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal

If device usage is inside of specified operating temperature (ambient temperature), power derating, and voltage, it is not detected as fault as long as the product is not defective.

(2) Detection pattern⑥(outside condition usage against specified)

There might be possibility to detect as fault in below state, loss exceeds the allowable state or ambient temperatures above 125℃, load larger than the specified connection or larger than the specified voltage, in the situation raises heat departing from the specification.

(3) Detection pattern⑦(IC Corruption)

If there is a situation such as excessive current flows through the internal IC due to some failure, it might be detected as fault.

8.5 Fault Detection Contents and Error Code

Error code was assigned for each fault. When fault is detected, error state output from "ERR"and "ERRHLD" terminals and ERRC1~3 will be output from the contents detected as an error code. In case of simultaneous errors, only the error code with priority is indicated.

■Error code(Result of failure detection) list

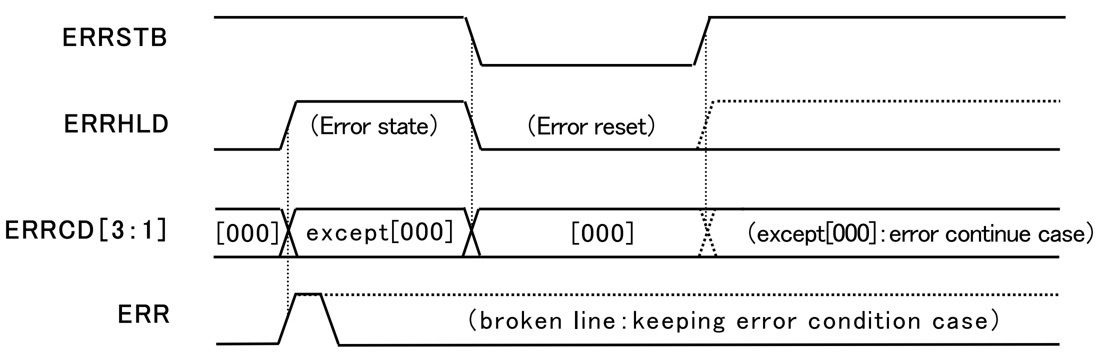
ERR CD3	ERR CD2	ERR CD1	Error Contents (Failure Detection result)	Priority※	Note
0	0	0	Normal	—	No error
0	0	1	Resolver signal abnormality	3	
0	1	0	Disconnection Detection(COS side)	1	
0	1	1	Disconnection Detection(SIN side)	2	
1	0	0	R/D conversion abnormality	4	
1	0	1	(Undefined)	—	
1	1	0	IC abnormal high temp(about over 150℃)	5	
1	1	1	Error Mask on start-up (After Reset release)	—	

※ Smaller numbers are getting higher priority.

8.6 Error Reset

The contents of "ERRHLD" and error code (ERRCD1~3) which is set by detecting fault can be reset by setting"ERRSTB=Low".

■Error-reset operation waveform



※ For timing detail, please refer 10.9 .

※ The ERRHLD output should be used after the error is reset by the ERRSTB input. When the ERRHLD output can not be released by the Error Reset, remove the true cause of error referring to the section 9.1.

9. If you think trouble shooting

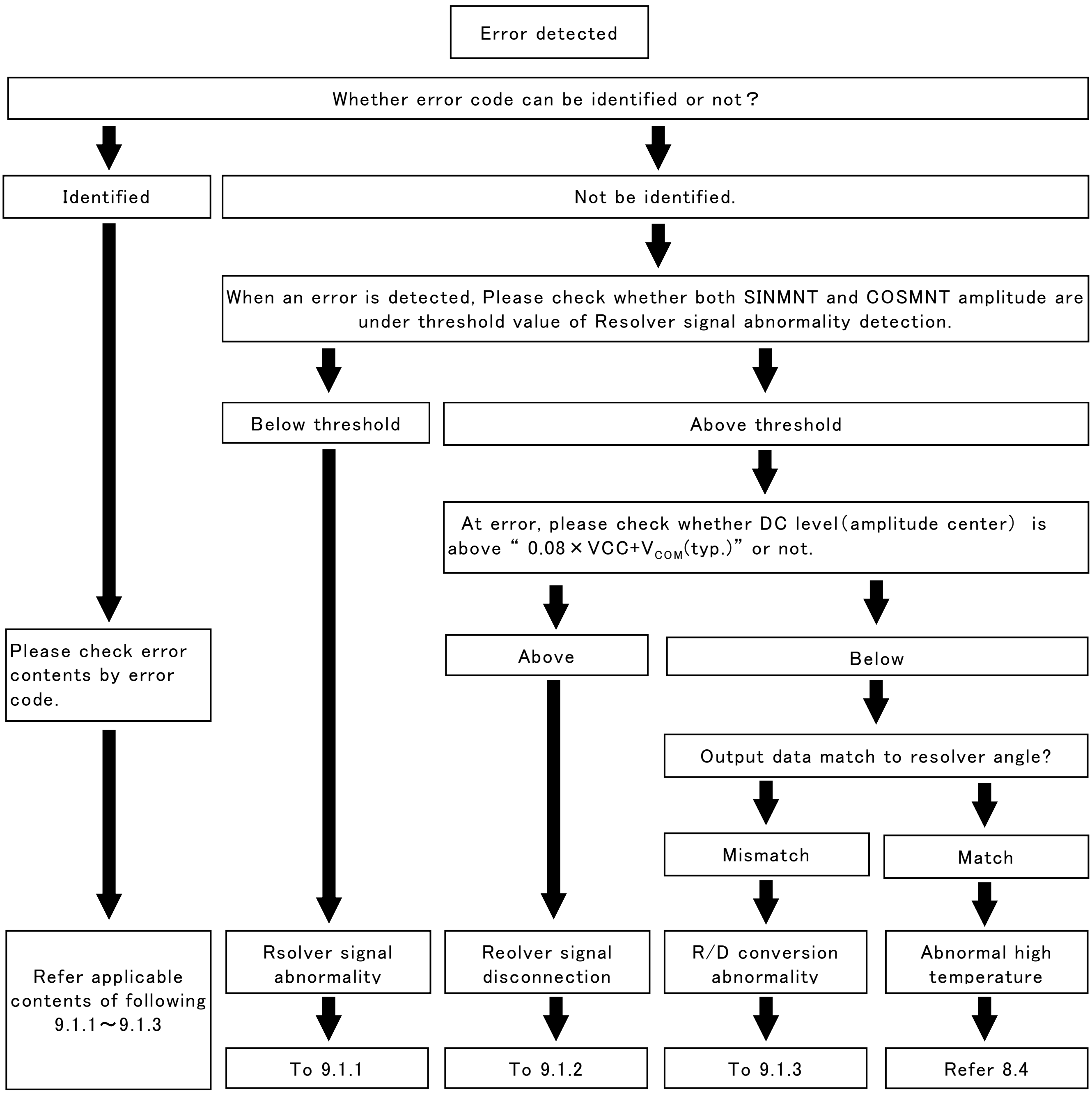
In this chapter, there are corresponding examples for the case of error detected by the function of fault detection, and for the case of strange angle output data. Please check these examples for your troubleshooting and operation check.

※Pleae note that there are cases where improvements can not be obtained even if making troubleshooting described in this chapter.

9.1 In case of error detection

When an error is detected (ERR or ERRHLD output are “H” level), refer to the following troubleshooting flow. Firstly please perform to estimate reason of fault detection, and error factor should be identified and eliminated according to the procedure of chapter 9.1.1 or lator. Regarding the operation of fault detection function, please refer chapter 8.

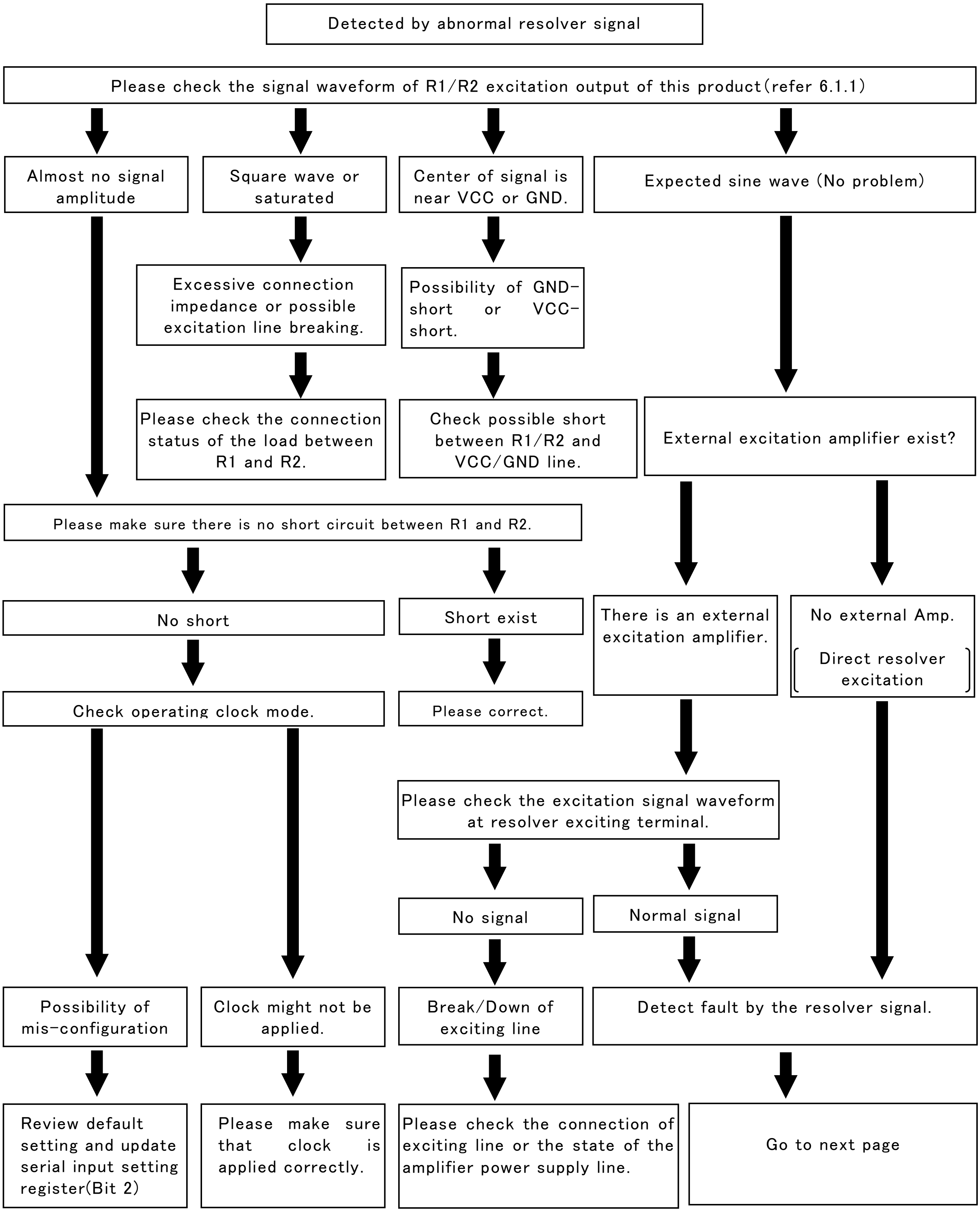
■Troubleshooting flow of error



9.1.1 Suspicion of Abnormal Resolver Signal

In case of suspicion of abnormal resolver signal detection, true error factor should be identified and eliminated according to the below troubleshooting flow.

■Troubleshooting flow of abnormal resolver signal



Detect fault by the resolver signal(Continue from previous page)

When the resolver rotation, please check whether SINMNT/COSMNT amplitude change or not.
(refer 6.1.2(1))

Amplitude is changing.

Please adjust the level of the monitor output(Refer 4.2.2)

Certain amplitude but no change

Please check the connection status.(Refer 5.1)

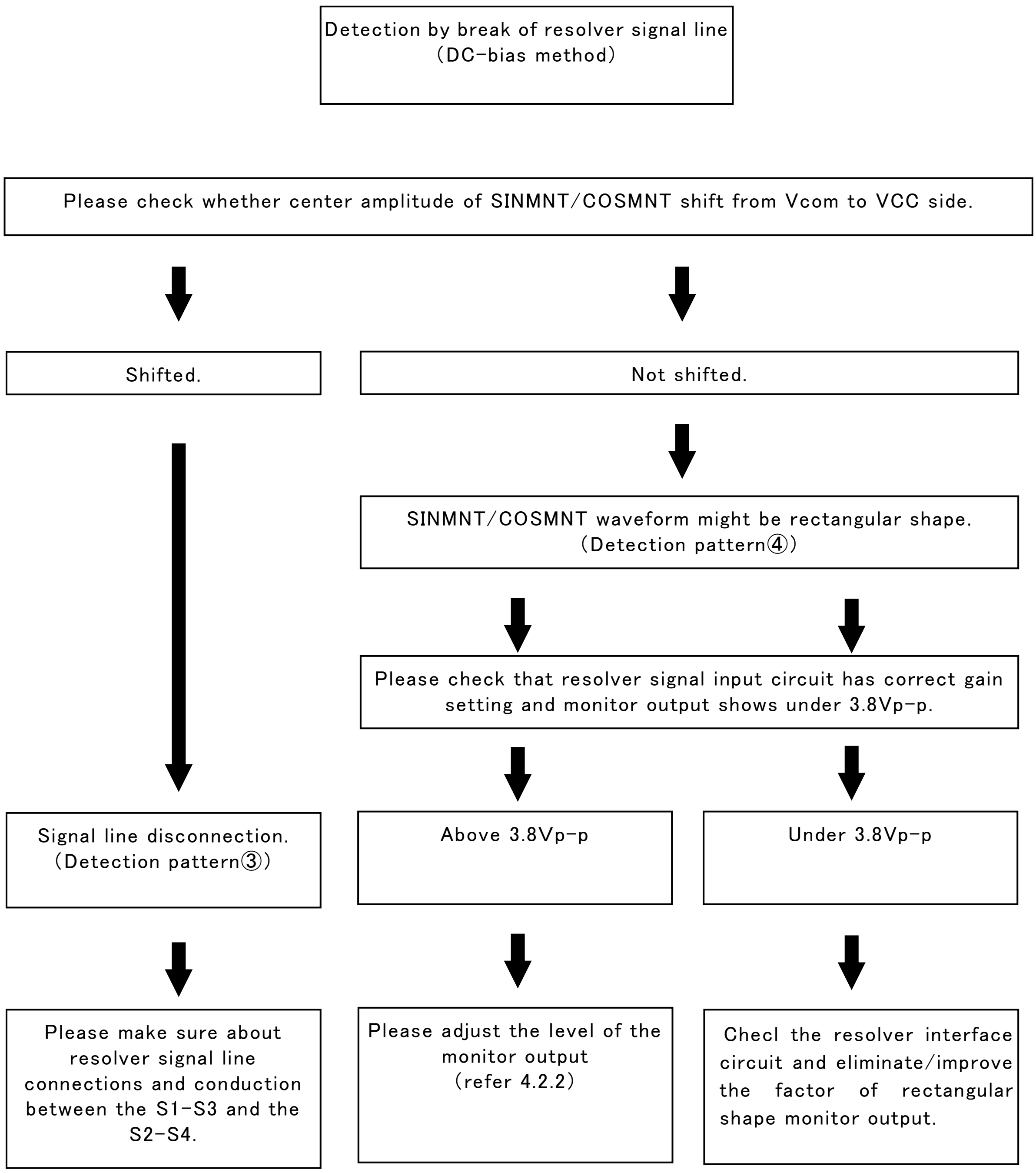
One monitor looks OK but the other one have no amplitude.

Please make sure there is no shorted line between each signal line and power(VCC/GND) line.

9.1.2 Suspicion of Disconnection Detection (DC-bias method)

In case of suspicion of disconnection detection of resolver signal line (DC-bias method), true error factor should be identified and eliminated according to the below troubleshooting flow.

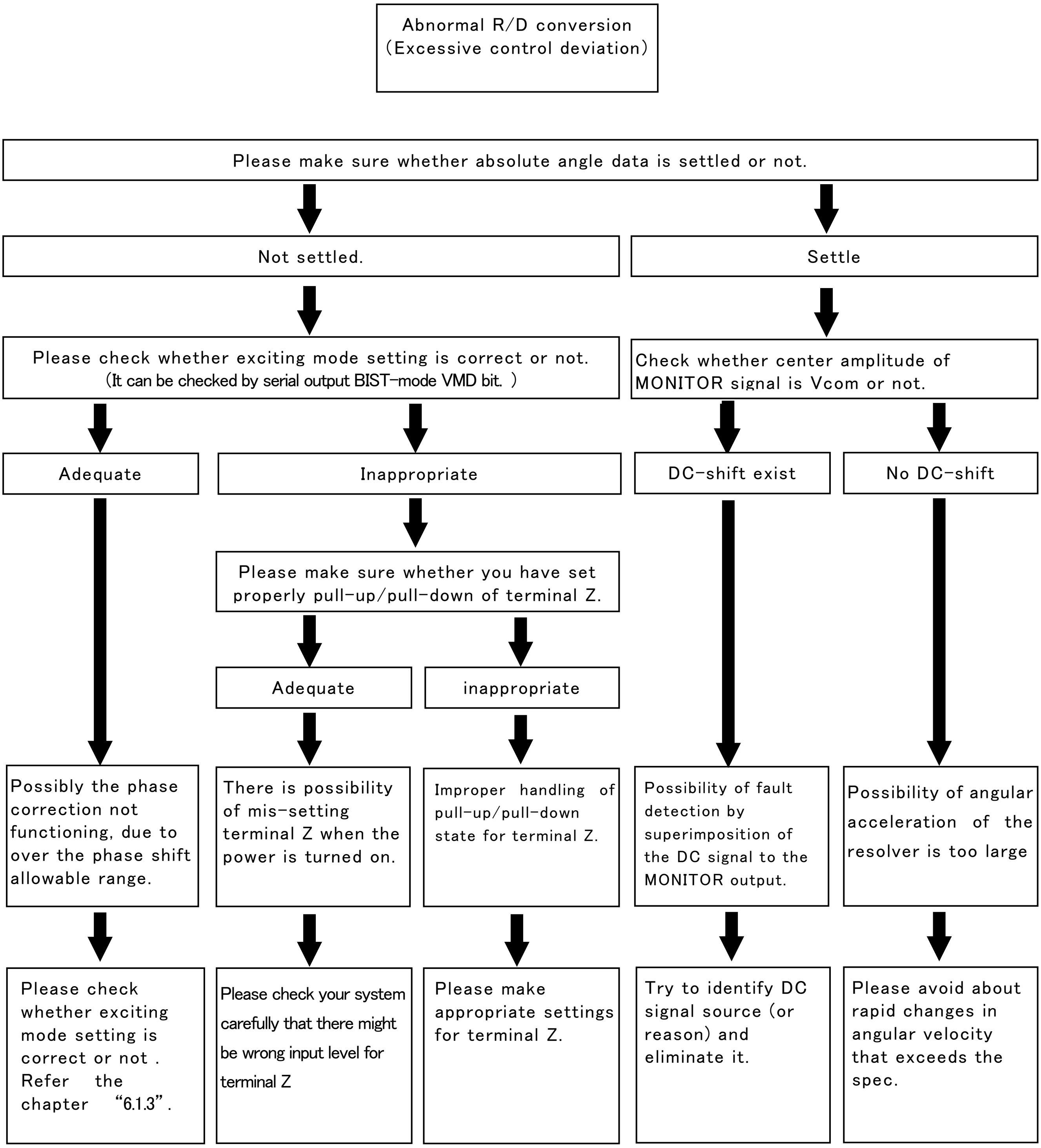
■Troubleshooting flow of detecting disconnection of resolver signal line.



9.1.3 Suspicion of Abnormal R/D conversion

In case of suspicion of abnormal R/D conversion, true error factor should be identified and eliminated according to the below troubleshooting flow.

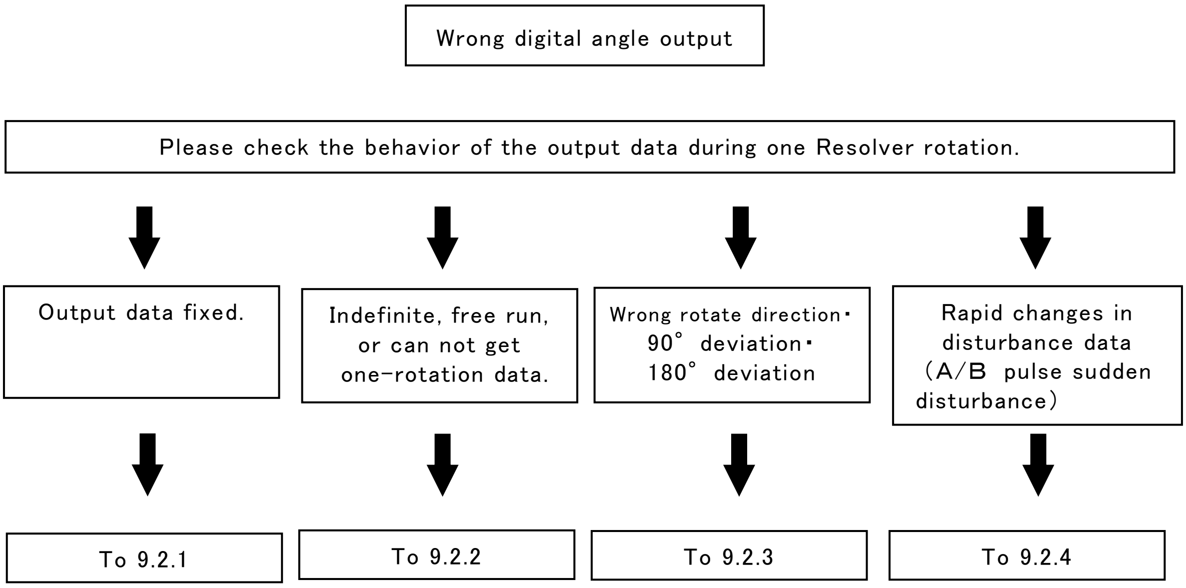
■Troubleshooting flow for abnormal R/D conversion detection



9.2 In case of wrong angle data

Despite the rotating Resolver, angle output data is not changed, or output shows the different format data, or output data is not fit to actual angle. In such case, please follow below troubleshooting flow and identify the behavior of the output data. Then please improve this error condition by the procedure described in chapter 9.2.1 and later.

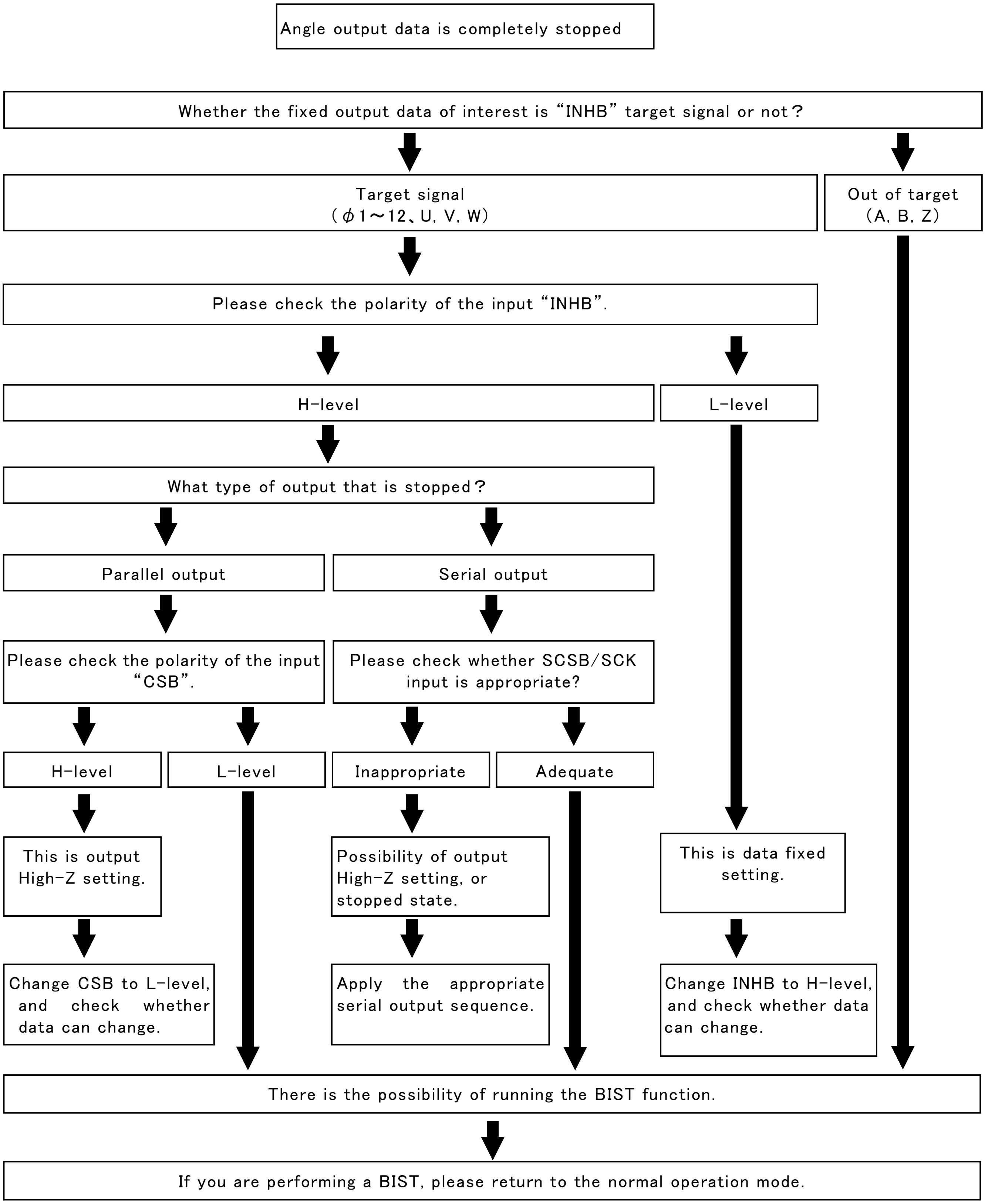
■Troubleshooting flow of wrong digital angle data.



9.2.1 In case of fixed angle data

In case of angle output data is completely stopped, please follow below troubleshooting flow and identify the factors, and then improve your system.

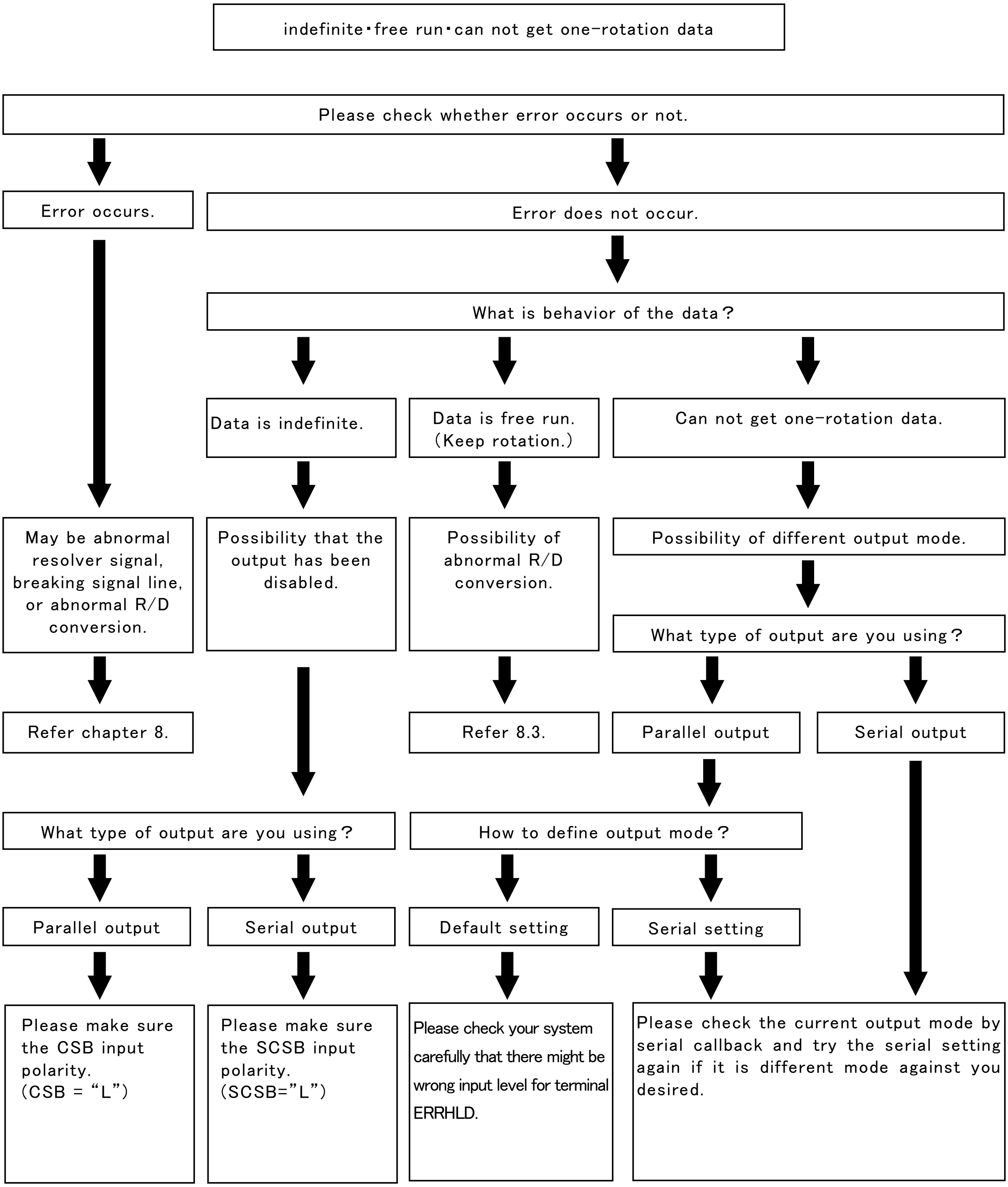
■Troubleshooting flow of fixed angle data



9.2.2 In case of indefinite, free run, can not get one-rotation data

In case of angle output data is indefinite, free run, can not get one-rotaion data, please follow below troubleshooting flow and identify the factors, and then improve your system.

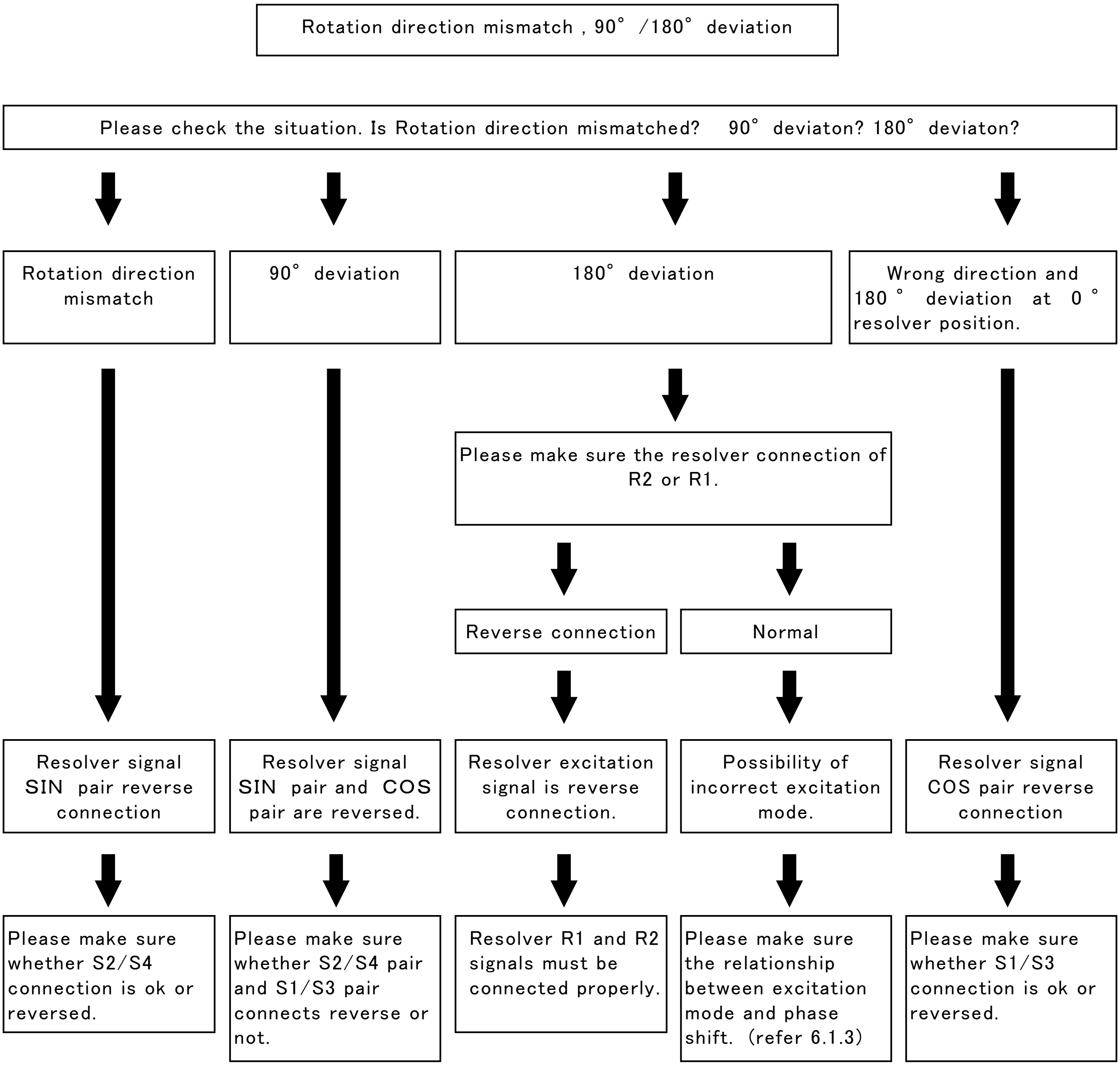
■Troubleshooting flow of indefinite, free run, can not get one-rotation data



9.2.3 In case of rotation direction difference, 90° deviation or 180° deviation

In case of angle output data shows rotation direction difference, 90° deviation or 180° deviation, please follow below troubleshooting flow and identify the factors, and then improve your system.

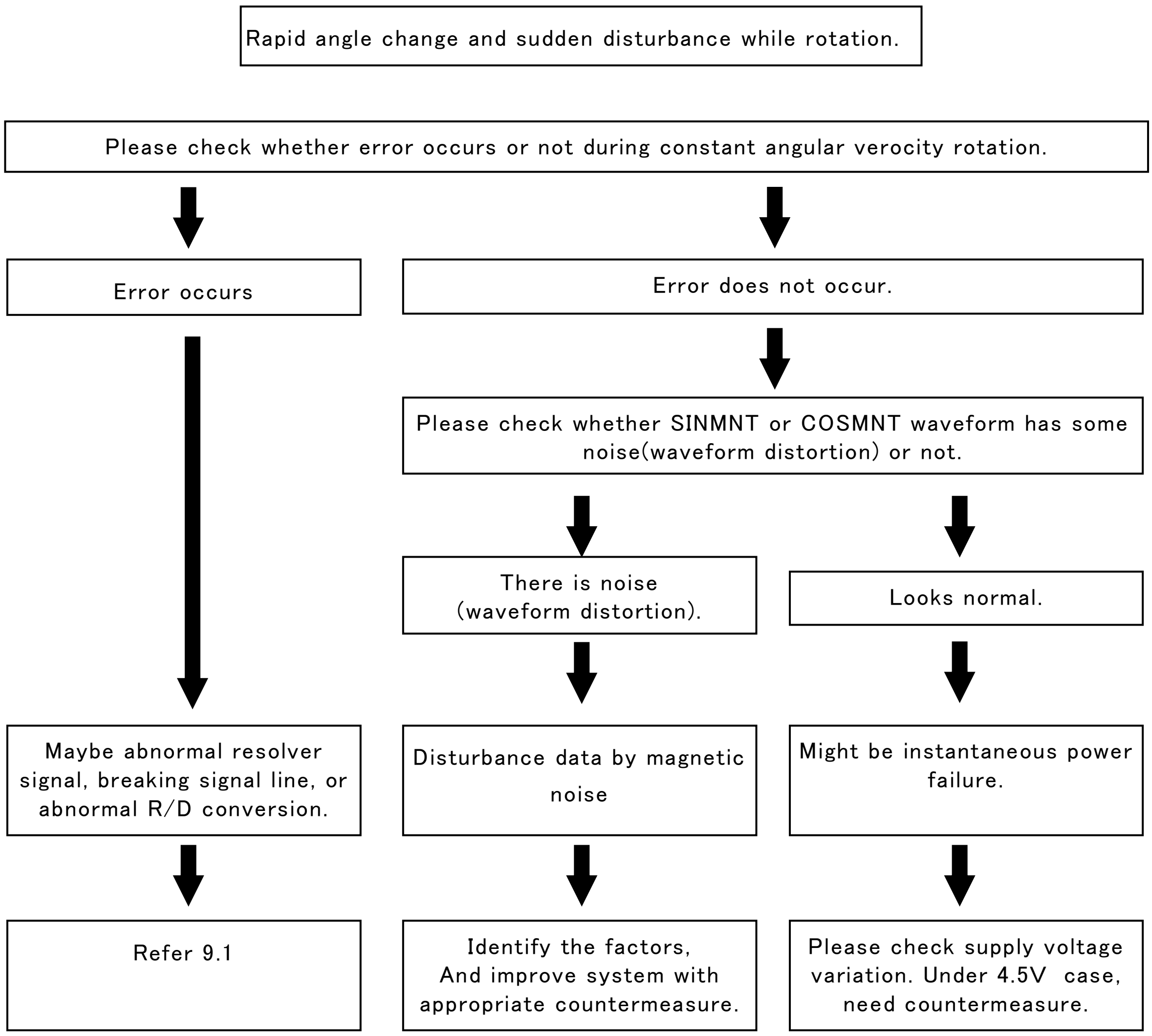
■Troubleshooting flow of rotation direction mismatch, 90° /180° deviation



9.2.4 In case of rapid change in the output angle data and disturbance

In case of rapid change in the output angle data or a sudden disturbance while rotation, please follow below troubleshooting flow and identify the factors, and then improve your system.

■Troubleshooting flow of rapid change in the output angle data and disturbance



9.3 If the situation does not improve

If the situation does not improve even if section 9.1 or 9.2 steps perform, and if there is another phenomenon which does not mention in this manual, please contact us with waveforms when an error occur (appropriate abnormal signal, SINMNT, COSMNT) and also inform us about detail troubled circuit information.

10. Electrical characteristics

10.1 Absolute maximum rating

Items	Symbol	Absolute maximum rating	Unit
Power supply voltage	VCC	−0.3～+6.5	V
	VRR	−0.3～+6.5	V
	VDD	−0.3～+6.5	V
Digital input voltage	Vin_d	−0.3～VDD+0.3	V
Analog input voltage (pin5～11)	Vin_a1	−0.3～VCC+0.3	V
Analog input voltage (pin13,15)	Vin_a2	−0.3～VRR+0.3	V
Voltage difference between VCC and VRR ※1	VCC−VRR	−0.3～+0.3	V
Voltage difference between GND sources.	AGND−RGND	−0.1～+0.1	V
	RGND−DGND	−0.1～+0.1	V
	DGND−AGND	−0.1～+0.1	V
Operating temperature	T_{opr}	−40～+125	℃
Storage temperature	T_{stg}	−65～+150	℃
Maximum power consumption	P_D	390	mW

※1 Include power−on situation and power−down situation.
※2 If you use the IC beyond the absolute maximum rating, it may cause permanent damage to the IC.

10.2 Power−related characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and condition
Power supply voltage	VCC	4.5	5.0	5.5	V	Recommended power supply voltage VCC, VRR, VDD must be used at the same potential.
	VRR	4.5	5.0	5.5	V	
	VDD	4.5	5.0	5.5	V	
Reset release voltage	Vrsth	3.4	−	4.4	V	Power−On−Reset release voltage
Reset voltage	Vrstl	3.2	−	4.2	V	Power−On−reset voltage
Reset voltage hysteresis	Vrhys	−	0.2	−	V	Vrsth−Vrstl
Supply current※	$I_{CC}1$	−	−	45	mA	RLV=H
	$I_{CC}2$	−	−	65	mA	RLV=L

※ Internal current consumption with no load condition of digital output , include exciting current.

10.3 R/D conversion characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Resolution			12		Bit	A number of divisions per electrical angle one rotation.
Conversion accuracy		−4	−	4	LSB	Absolute error of the electrical angle input in a stationary state.(At 12Bit accuracy)
Settling time (Electrical angle 180° input step. Setting range: within ±8LSB)			42		Ms	Loop gain: Fixed value① (Bandwidth 800Hz)
			17		Ms	Loop gain: Fixed value② (Bandwidth 2,000Hz)
			14		Ms	Loop gain: Fixed value③ (Bandwidth 2,500Hz)
			24		Ms	Loop gain: Fixed value④ (Bandwidth 1,500Hz)
			35		Ms	Loop gain: Fixed value⑤ (Bandwidth 1,000Hz)
			69		Ms	Loop gain: Fixed value⑥ (Bandwidth 500Hz)
			170		Ms	Loop gain: Fixed value⑦ (Bandwidth 200Hz)
			1.5		Ms	Loop gain: Auto-tuning
Maximum angular velocity (Angular velocity range capable of tracking (electorical angle))		240,000			min^{-1}	Loop gain: Fixed value setting
		12,000			min^{-1}	Loop gain: Auto-tuning setting
		15,000			min^{-1}	Serial absolute output 16BIT setting
		12,000			min^{-1}	Serial absolute output 16BIT setting and Auto-tuning setting
Maximum angular acceleration (Angular acceleration range capable of tracking (electorical angle))			230,000		rad/s^2	Loop gain: Fixed value① (Bandwidth 800Hz)
			1,110,000		rad/s^2	Loop gain: Fixed value② (Bandwidth 2,000Hz)
			1,370,000		rad/s^2	Loop gain: Fixed value③ (Bandwidth 2,500Hz)
			800,000		rad/s^2	Loop gain: Fixed value④ (Bandwidth 1,500Hz)
			290,000		rad/s^2	Loop gain: Fixed value⑤ (Bandwidth 1,000Hz)
			70,000		rad/s^2	Loop gain: Fixed value⑥ (Bandwidth 500Hz)
			7,000		rad/s^2	Loop gain: Fixed value⑦ (Bandwidth 200Hz)
			3,000,000		rad/s^2	Loop gain: Auto-tuning
Responsibility		−0.2		0.2	deg./ 10,000min^{-1}	Output response delay in a constant angle velocity (Equivalent to 3.3 μs)
Stabilizing time at start				20	ms	Stabilizing time of output at power-on. (±8LSB max at static state)

10.4 Built-In Self-Test(BIST) characteristic

items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
R/D conversion BIST(0°)						
Detection judgment threshold		−1.4	−	1.4	deg.	Allowable range for the setting angle
Detection time		−	−	10	ms	The time required to stabilize BIST results.
R/D conversion BIST(45°)						
Detection judgment threshold		−1.4	−	1.4	deg.	Allowable range for the setting angle
Detection time		−	−	10	ms	The time required to stabilize BIST results.
R/D conversion BIST(270°)						
Detection judgment threshold		−1.4	−	1.4	deg.	Allowable range for the setting angle
Detection time		−	−	10	ms	The time required to stabilize BIST results.
Resolver signal abnormality BIST						
Detection time		−	−	0.5	ms	The time required to stabilize BIST results.
Resolver signal disconnection BIST						
Detection time		−	−	1	ms	The time required to stabilize BIST results.
R/D conversion abnormality BIST						
Detection time		−	−	10	ms	The time required to stabilize BIST results.

10.5 Failure detection characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Resolver signal abnormality						
Detection threshold 1		0.1× V_{CC}−5%	−	0.1× V_{CC}+5%	Vp-p	Setting register Bit12 = 0 case. Compared with resolver signal monitor output amplitude※1
Detection threshold 2		0.14× V_{CC}−5%	−	0.14× V_{CC}+5%	Vp-p	Setting register Bit12 = 1 case. Compared with resolver signal monitor output amplitude※1。
Relative deviation between range		0.04× V_{CC}−5%	−	0.04× V_{CC}+5%	Vp-p	Threshold_2 − Threshold_1
Detection time		−	−	0.5	ms	Time required detecting fault. ※2
Resolver signal disconnection (DC-Bias Method)						
Detection threshold 1		0.08× V_{CC}−5%		0.08× V_{CC}+5%	V_{DC}	Except setting as follows Compared with resolver signal monitor DC-level ※3
Detection threshold 2		0.35× V_{CC}−5%		0.35× V_{CC}+5%	V_{DC}	DCMDB=L and EXMDB=H Compared with resolver signal monitor DC-level ※3
Detection time		−	−	10	ms	Time required detecting fault ※2
R/D conversion abnormality (Excessive control deviation)						
Setting threshold High		0.55× V_{CC}−5%		0.55× V_{CC}+5%	V_{DC}	Compared with the internal control deviation voltage ※4
Setting threshold Low		0.45× V_{CC}−5%		0.045× V_{CC}+5%	V_{DC}	Compared with the internal control deviation voltage ※4
Detection time		−	−	10	ms	Time required detecting fault ※2 ※5

※1 If both SINMNT and COSMNT become within the threshold, it is judged as abnormal.
※2 In case of the continuous time of failure is shorter than above detection time, there is possibility not to detect failure.
※3 If DC level variation become more than threshold, it is judged as abnormal.
※4 If error deviation is more than threshold in the High side or less than one in the Low side, it is recognized as excessive.
※5 If control variation recognition rate as too much is more than 50% as around 5.9ms duration, it is judged as abnormal.

10.6 Analog signal characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Excitation output						
Output current 1		7	10	13	mArms	RLV=H
Output current 2		14	20	26	mArms	RLV=L
Output frequency 1		7	10	13	kHz	Frequency range when using the internal clock
Output frequency 2			f_{CLK}/ 1,000		Hz	Frequency by external clock. (f_{CLK}= external clock frequency)
Load impedance 1				200	Ω	Allowable load impedance of R1/R2. RLV=H
Load impedance 2				100	Ω	Allowable load impedance of R1/R2. RLV=L
Resolver signal input						
Input protection resistor		–	360	–	Ω	
Input amplifier feedback resistor	R_F	16.8	21	25.2	kΩ	
Relative accuracy of above resistor		−1	–	1	%	
Career gain		−20	–	20	%	The variation of monitor output voltage when resolver is directly excited by the R1/R2 of this IC.※
Resolve signal monitor output						
Internal reference voltage	V_{COM}		VCC/2		V	SINMNT, COSMNT terminal center voltage.
Max output amplitude		3.8	–	–	Vp-p	
Load impedance		20	–	–	kΩ	Allowable load impedance of SINMNT and COSMNT.

※ Except the tolerance of input resistances and peripheral circuit, the performance of resolver itself.

10.7 DC characteristics of digital signal

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
High level input voltage	V_{IH}	0.8×VDD	–	VDD	V	Recommended input "H" voltage for all digital input terminals.
Low level input voltage	V_{IL}	0	–	0.2×VDD	V	Recommended input "L" voltage for all digital input terminals.
Input hysteresis voltage	V_H	0.36	–	–	V	
Input pull-up resistance 1	R_{PU}	30	50	85	kΩ	Pull-up resistor value of digital input. (Applicable terminals: SSDT, SSCS, SCSB, SCK, CSB,, INHB(RD), ERRSTB, CLKIN, BISTVLD, EXMDB, DCMDB, RLV, PUPD, TEST1)
Input pull-up resistance 2	R_{PUBI}	72	120	200	kΩ	Pull-up resistor value of digital input. (Applicable terminals: ERRHLD, ERR, Z)
Input pull-down resistance	R_{PL}	30	50	85	kΩ	Pull-down resistor value of digital input. (Applicable terminal: TEST2)
Input leakage current ※	I_L	–	–	-200	μA	V_I=DGND
High level output voltage	V_{OH}	VDD-0.1	–	–	V	I_{OH}=0mA
Low level output voltage	V_{OL}	–	–	0.1	V	I_{OL}=0mA
High level output current	I_{OH}	-4	–	–	mA	V_{OH}=VDD-0.5V
Low level output current	I_{OL}	4	–	–	mA	V_{OL}=0.5V

※Input leak current definition. "－"direction means outflow.

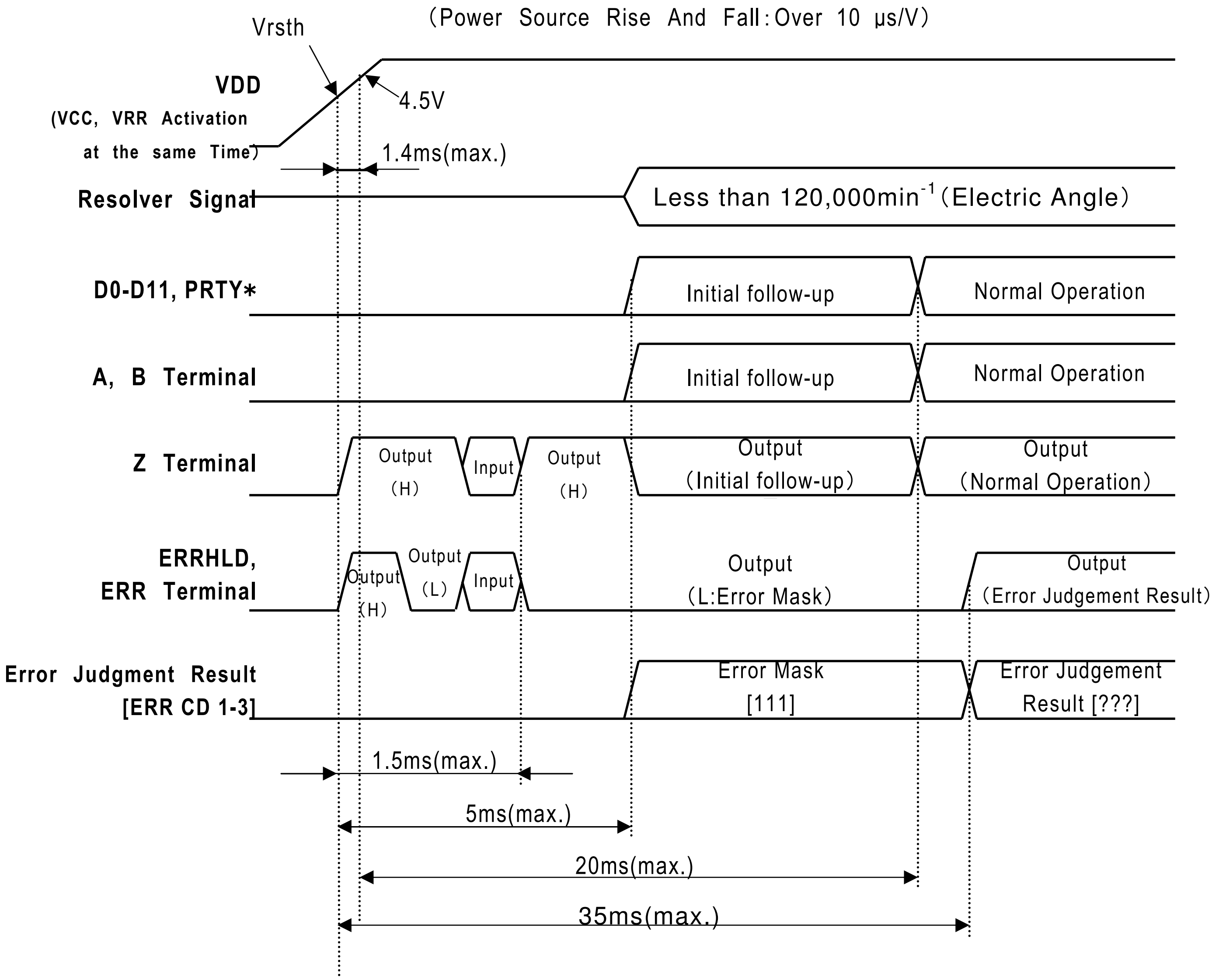
10.8 AC characteristics of digital signal

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
External CLK input frequency	F_{EXTCLK}	7	10	13	MHz	
External CLK duty	D_{EXTCLK}	40	–	60	%	
Internal digital CLK frequency	F_{INTCLK}	35	50	65	MHz	
Serial CLK input frequency	F_{SCK}	–	–	5	MHz	
Input rise-up time※	tri	0	–	1.0	ms	
Input fall-down time※	tfi	0	–	1.0	ms	
Output rise-up time	tr	–	–	6	ns	C_L=15pF
Output fall-down time	tf	–	–	6	ns	C_L=15pF

※Output rise-up time /output fall-down time means the transition time of the range 0.2VDD～0.8VDD.

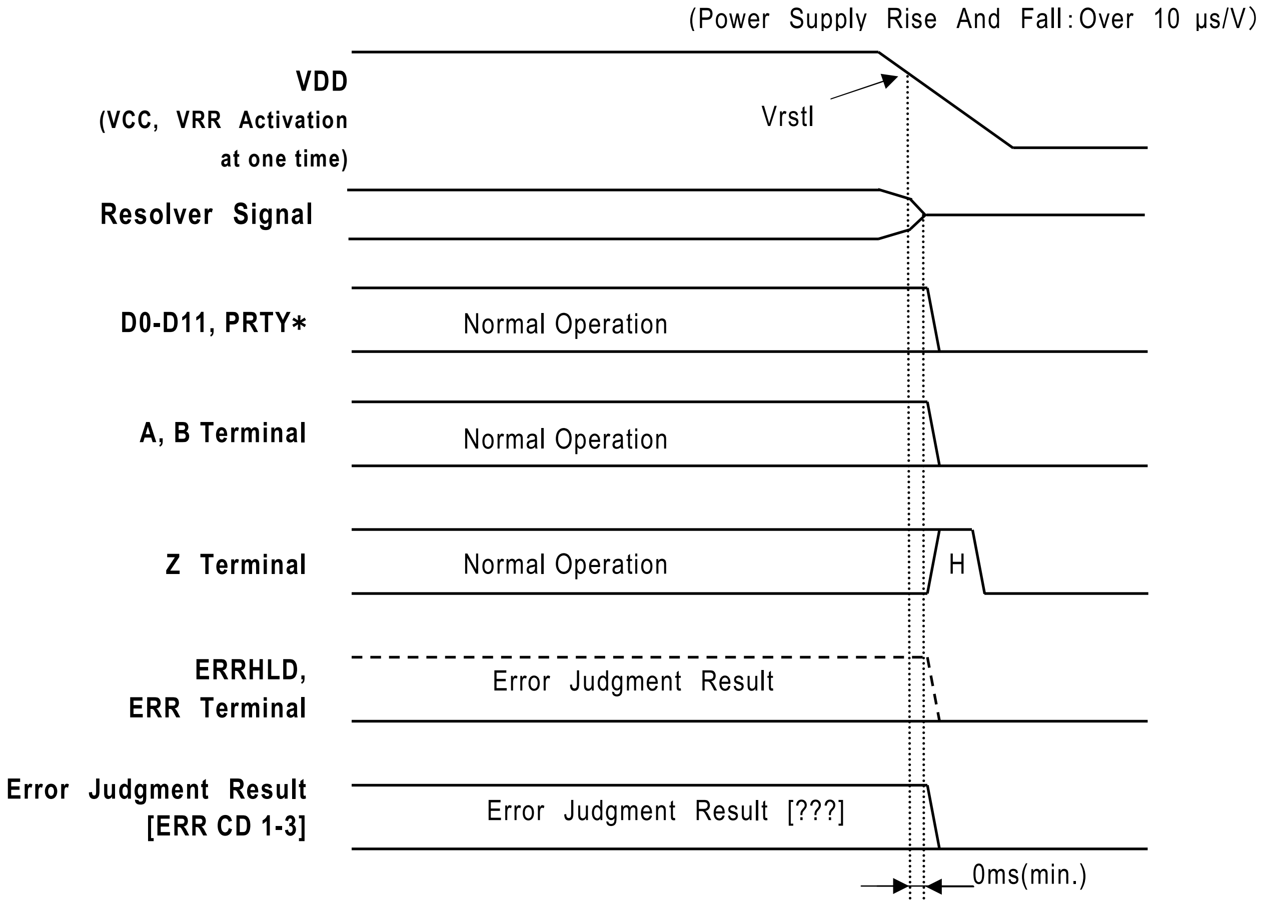
10.9 Timing diagram

■ Power-on sequence



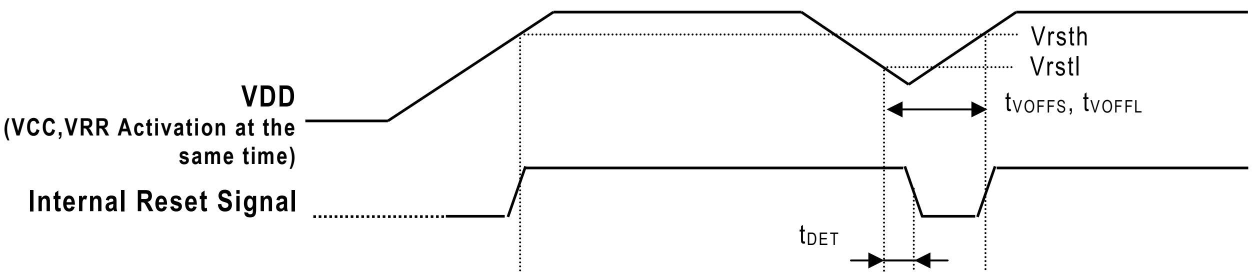
* D0-D11, PRTY output validity depends on CSB

■ Power-off sequence



* D0-D11, PRTY output validity depends on CSB

■ Timing of internal reset signal

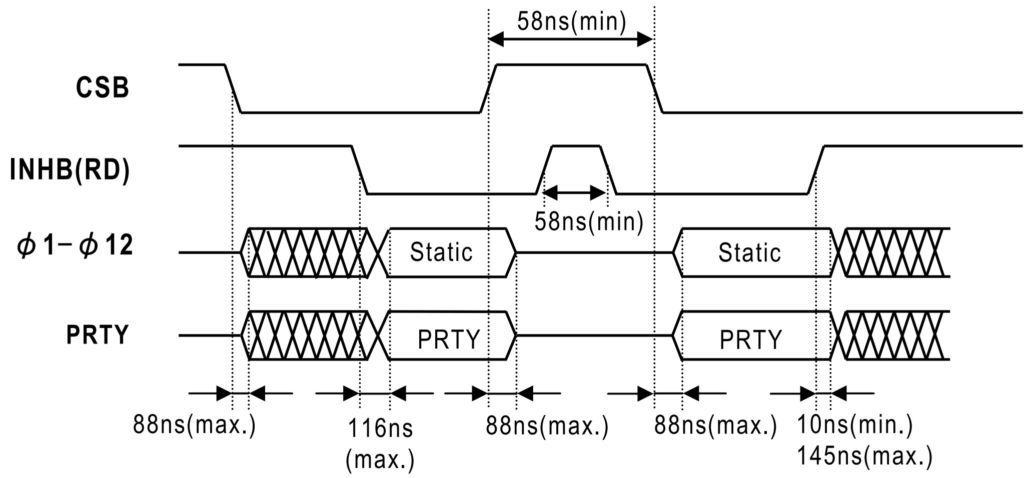


Code	Specification Value[ms]			Note
	Min.	Typ.	Max.	
T_{DET}	0.5		3.0	Relay Delay Time
T_{VOFFS}			0.5	Reset Disable VDD Decreasing Time(Note 1)
T_{VOFFL}	3.0			Rest Enable VDD Decreasing Time(Note 2)

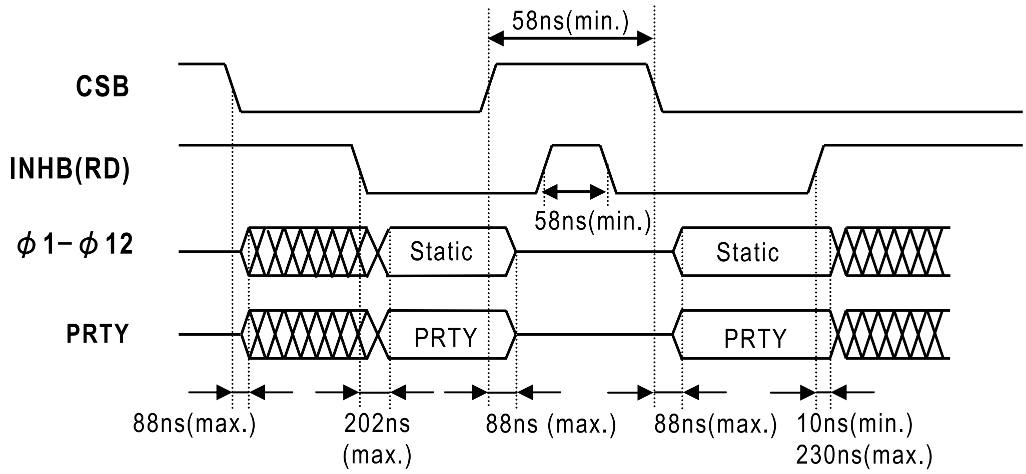
(Note 1) Maximum VDD Decreasing Time with reset
(Note 2) Minimum VDD Decreasing Time with reset

■ Timing of Bus Control

- Bus control timing in “PUPD=1” -

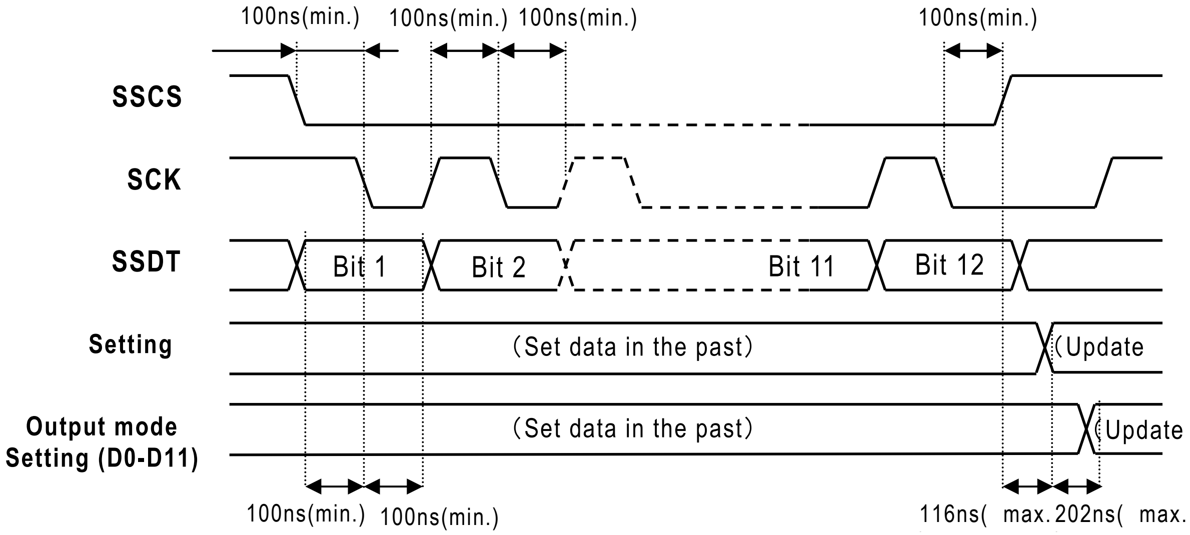


- Bus control timing in “PUPD=0” -

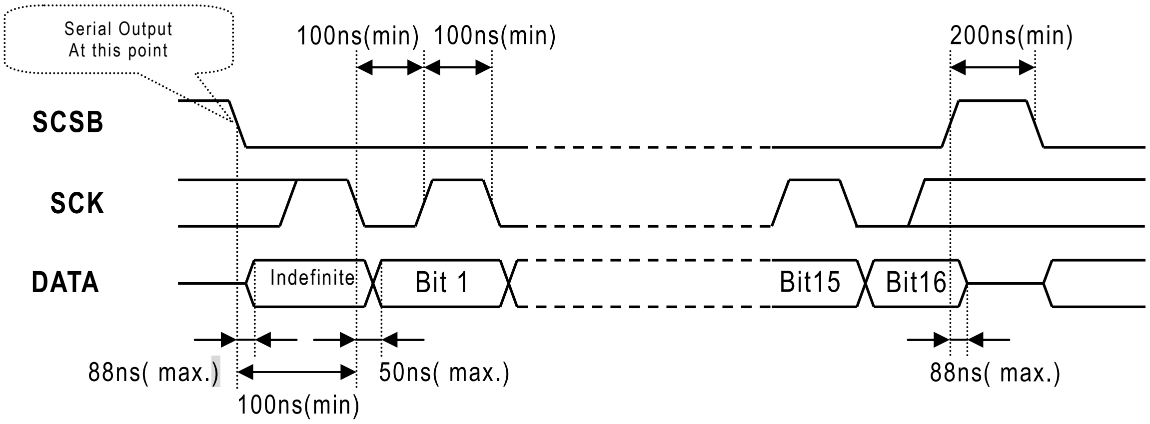


■ Serial input setting sequence

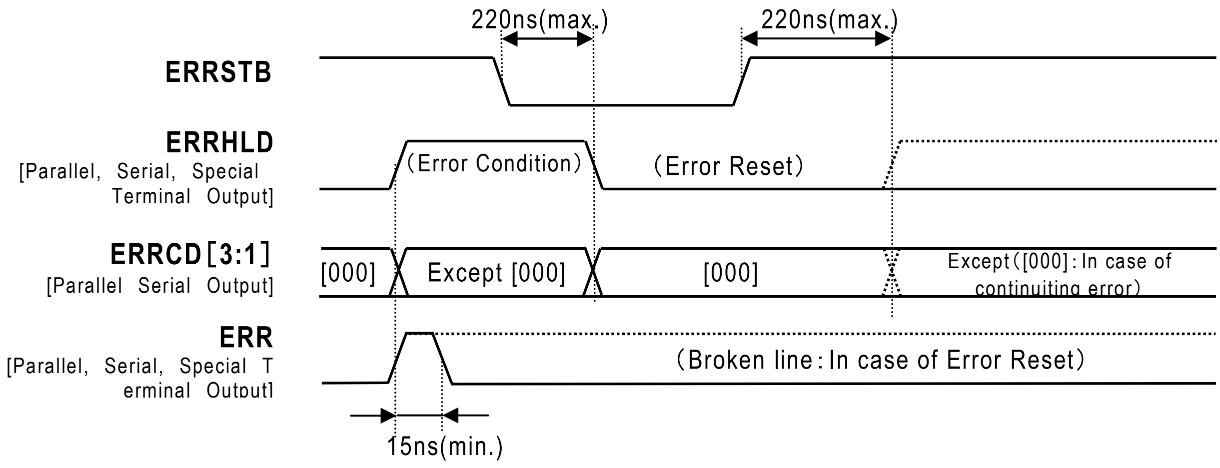
※1　Do not perform serial input set sequence during 5ms after start up or reset(reboot).



■ Serial output sequence

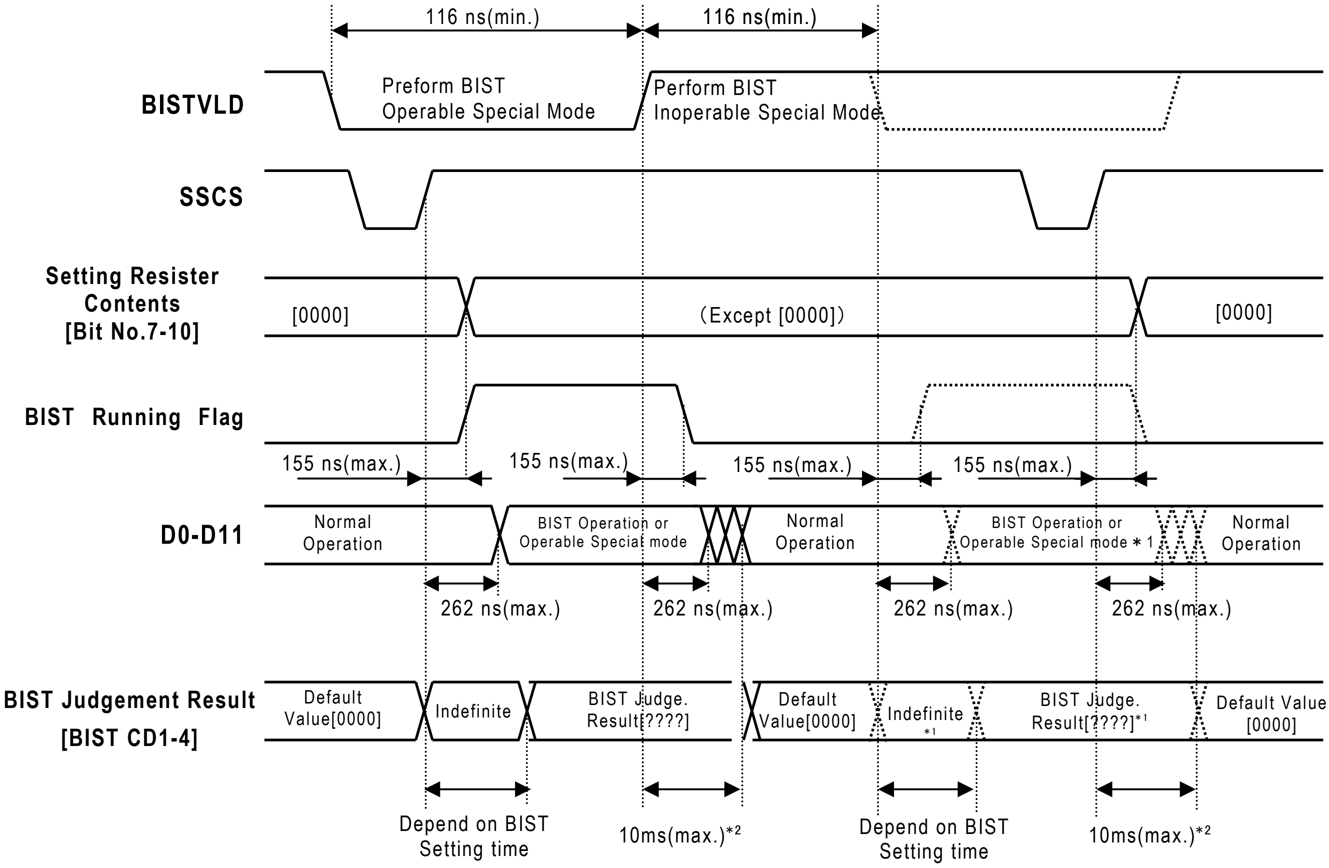


■ Timing of Error Reset



※1 Please use ERRHLD output after the error is reset by ERRSTB input certainly.
If ERRHLD output error cannot be reset, eliminate true error factor.
※2 Parallel and serial signal output is covered in INHB(RD).
※3 Sequence specified in Figure 5 is necessary to load signal related serial output error.

■ Operating sequence of Built-in Self-test(BIST)



※1 Broken line means BISTVLD=L except setting resister [Bit No.7-10]=[0000]
※2 less 120,000min^{-1}(electric angle)
※3 Don't run serial input/output sequence in 116ns before/after BISTVLD polarity switch.
※4 Angular velocity should be below 7,500 min^{-1}(electric angle), between 10ms after 16 bit mode setting of serial absolute output.

Built-In Self Test(BIST) and special mode can run only during “BISTVLD” input is capable to run as “Low” and Built-In Self Test(BIST) and special mode in setting register. In addition, system reset can issue when SSCS=H.

11. Appendix

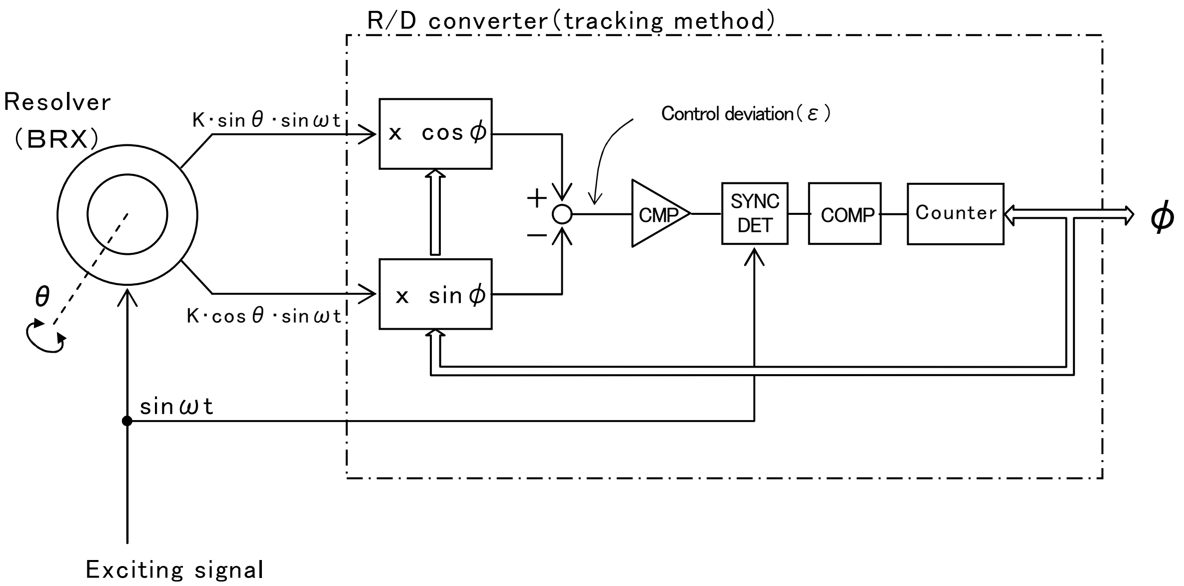
11.1 R/D conversion principle

This product adopted digital tracking method as R/D conversion system, and this method is one of the negative feedback control of closed-loop configuration, then it convert from Resolver analog signal to digital signal. A control deviation(ε) is shown in below equation, and it must be normally "0" with the negative feedback control system.

$$\text{Control deviation} \; : \; \varepsilon = K \cdot \sin(\theta - \phi) \cdot \sin\omega t$$

Here assuming "$\varepsilon = 0$" means "$\theta = \phi$", then Resolver analog angular signal can be converted to digital angular data.

■Configuration of digital tracking method R/D converter.



【Control deviation】: $\varepsilon = K \cdot \sin\theta \cdot \sin\omega t \times \cos\phi - K \cdot \cos\theta \cdot \sin\omega t \times \sin\phi$

$= K \cdot \sin(\theta - \phi) \cdot \sin\omega t$

$\varepsilon = 0 \quad \Rightarrow \quad \therefore \theta = \phi$

【Explanation of concept】

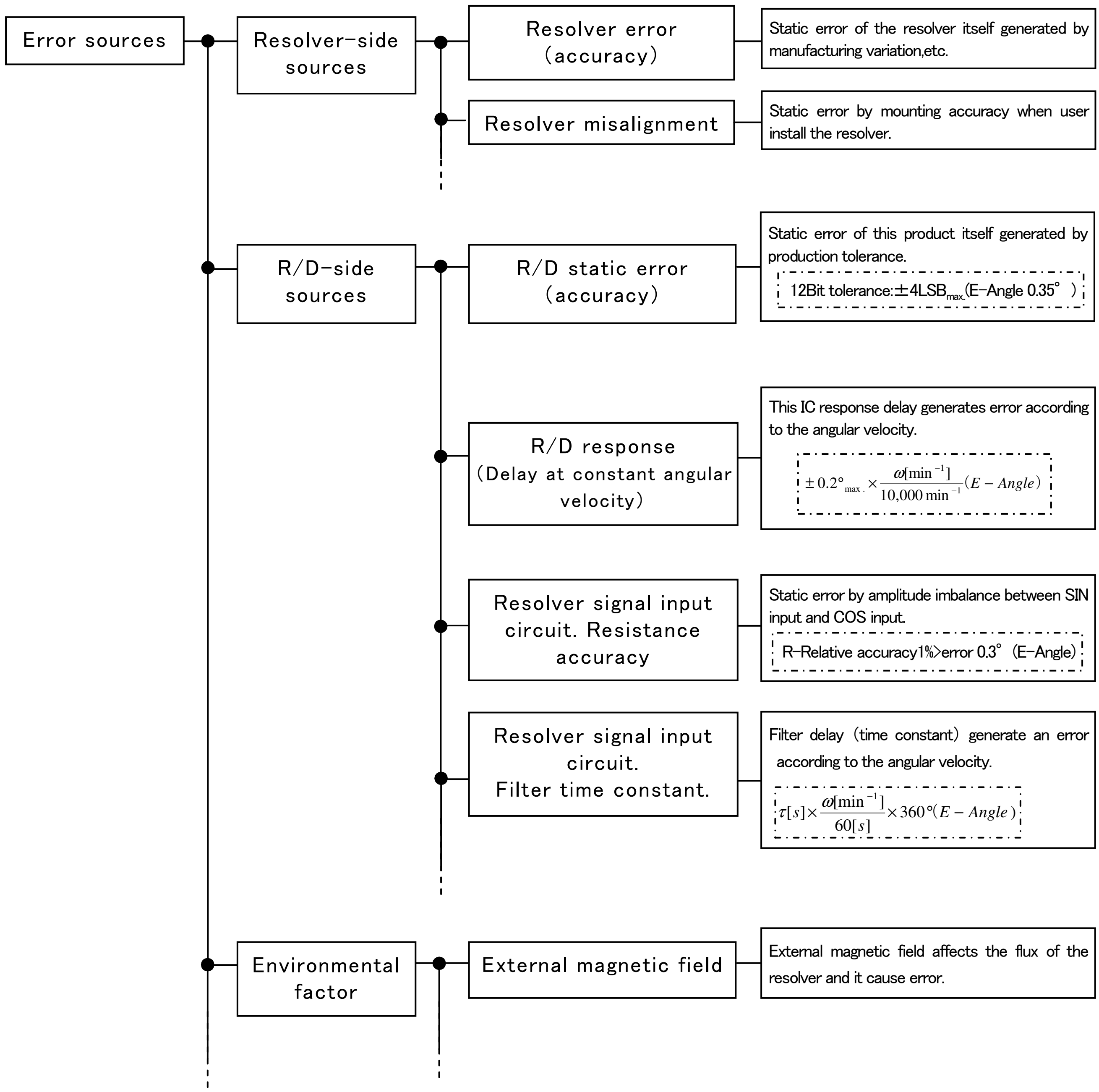
An amplitude modulated resolver signals enter to R/D converter. To caliculate control deviation (ε), $\sin\theta$ modulated signal is multiplied by feedback $\cos\phi$ and $\cos\theta$ modulated signal is multiplied by feedback $\sin\phi$. This "ε" is encoded by comparator (Analog to Digital conversion), and $\sin\omega t$ component is removed by synchronous detection. Through a compensator which stabilize negative feedback loop and improve its characteristic (In general, compensator is PI control which configure with type Ⅱ direct servo loop.) , digital angular output ϕ can be generated as counter value.

11.2 About the error of resolver system

Resolver system with this product causes an error against actual angular position by resolver accuracy, this smartcorder accuracy, peripheral configuration error, etc. In this chapter, explain the error sources of resolver system and general estimation method of total error.

11.2.1 Error sources

There are error souces of resolver system like the following.



11.2.2 Error estimates

Total error of the resolver system using this IC is a combination of potential errors which include static error that typically come from resolver itself or this IC itself, and proportional error of angular velocity that come from delay of this IC or peripheral circuit depending on the angular velocity.

$$\varepsilon_{TTL} = \varepsilon_{ST} + \varepsilon_{DLY} + \cdots$$

While ε_{TTL} : Total Error of resolver system
ε_{ST} : Static error of resolver system
ε_{DLY} : Angular velocity proportional error

※ Each error might have different unit, and there are concepts which are "Number of multiple", "Mechanical angle", "Electorical angle". (Refer section 11.4 for each term). When estimating the error, please be careful to fitting the unit.

■Estimation of static error

Considering the estimation method of resolver system static errors which include resolver accuracy and error of this IC itself and the variation of the peripheral circuit or configuration, the easiest way is taking the sum of the maximum error caused by factors. But it is difficult to assume a probability that all of errors will be worst value, considering process capability, etc. Also it might need excessive precision characteristic to satisfy system, and then system cost might lead to increase.

Then static error of resolver system estimates normally with root mean square (RMS) method.

$$\varepsilon_{ST} = \sqrt{(\varepsilon_R)^2 + (\varepsilon_S)^2 + (\varepsilon_{RD})^2 + (\varepsilon_i)^2 \cdots}$$

While ε_{ST} : Static error of resolver system
ε_R : Error of resolver
ε_S : Error of resolver misalignment
ε_{RD} : Static error of this IC itself
ε_i : Resolver signal input circuit :Resistance accuracy

■Estimation of angular velocity proportional error

Angular velocity proportional error of resolver system is caused by response delay of this IC and signal delay which depend on the filter circuit constructed in resolver input circuit. This error is getting bigger with higher angular velocity, and it is obtained by converting the angular displacement from total delay time at applied angular velocity. Then it is estimated as the sum of individual errors due to the delay factor.

$$\varepsilon_{DLY} = \varepsilon_{RDDLY} + \varepsilon_{FLTDLY} + \cdots$$

While ε_{DLY} : Angular velocity proportional error of resolver system
ε_{RDDLY} : Angle error of this IC response delay
ε_{FLTDLY} : Angle error of the filter time constant at resolver signal input circuit.

11.3 FAQ

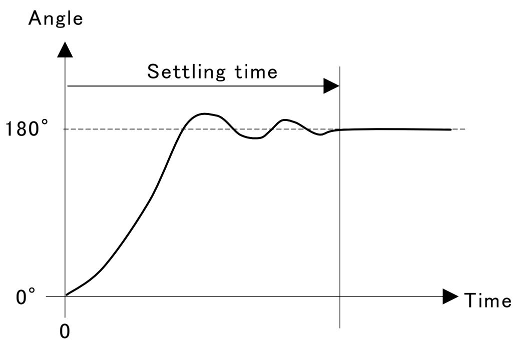
■Questions on the performance・characteristic of R/D conversion

Q	How much time it takes to convert R/D？
A	Assumed as delay time from input of resolver signal to output of its angle data. Then it will be 3.3μs max. Response spec is converted value from above time to the angular displacement while constant speed of rotation.

Q	What is the frequency (period) the output data is updated？
A	Except PUPD pin setting output : 25MHz(40ns)typ PUPD pin setting output (parallel absolute output): refer 4.3.1(3) .

Q	Explain a frequency response of negative feedback loop which realize R/D conversion.
A	Refer section 4.3.1(2)

Q	What happen the output data in case of resolver signal input is above maximum angular velocity?
A	R/D converter is not possible to work with the over-spec condition, then it can not follow the resolver rotation. A/B/Z pulse and angleΦ output show irrevant data (loss of synchronism condition).

<table>
<tr><td>Q</td><td>What is settling time？</td></tr>
<tr><td>A</td><td>The time to respond when resolver signal input change as step-like 180° . This is one of the indicators which show control system performance of R/D converter.
There is no chance to work this step(180°) response for the actual resolver signals.

</td></tr>
</table>

Q	In the operation of the rotating resolver, output angle data against actual resolver angle is shifted with the direction of rotation. Are there any considerable factor?
A	Typical factors are following. **(1) Displacement of the device which put on the resolver.** There might become angular displacement depending on direction, caused by mechanical misalignment of device like backlash of gear, etc. The problem of this factor is only depending on the rotation direction, and it is not depend on revolution speed of resolver. **(2) Time constant of filter circuit.** If resolver signal input to AU6805 through filters, there might show angular displacement depending on rotation direction while high speed resolver operation, caused by time constant delay value of filter circuit. The problem of this factor normally tends to be large in proportion to the number of revolution. **(3) AU6805 response （Delay time of response）** Delay time from resolver signal input to corresponding angular data output might cause of the deviation angle which depend on the direction at high speed resolver operation. The problem of this factor normally tends to be large in proportion to the number of revolution.

■Questions about the resolver interface.

Q	Is it possible to use this R/D converter without using the exciting signal output？
A	Set EXMDB=”L” (R1/R2 terminal set as external exciting signal input mode). Then it is possible to use external exciting signal which generate external source. For detail, please refer section 4.2.3 or 5 .

Q	A direct excitation function of the AU6805 output can not generate voltage of the resolver specification.
A	Direct excitation voltage is the product of resolver input impedance (RLV=“H” case is below 200Ω, RLV=”L” case is below 100Ω) and excitation output current. If you need a larger excitation voltage, you need to excitation via the external booster amplifier which source is AU6805 exciting output. It will be judged by considering noise effect whether we need to excitation resolver with the larger voltage or not. And it will not be always required such larger voltage amplitude.

Q	How does this affect if you connect a load of more than specification value between R1-R2 of AU6805?
A	There will be assumed that enough current can not flow in, the excitation signal is saturated, can not get normal waveform. In addition, signal amplitude will be smaller than the calculated value due to saturated signal.

Q	If we make short between R1-R2,　Will the AU6805 be broken？
A	There is no damage by overcurrent, etc because output is current control type.

Q	Please show us the voltage specification of R1-R2 input mode, when we use its terminals as external exciting signal input.
A	Input signal voltage range of each terminals must be -0.3～VRR+0.3V (absolute maximum rating specification) to prevent IC damage. Regarding the differential signals (R1-R2), it is operational while there is potential difference. But it is recommended to apply over 4Vp-p, because applying higher voltage will be getting better comparator sensitivity.

Q	What kind of behavior if you do not enter anything resolver signal？
A	It will be the situation that control loop is broken. Then the angles of the output data repeatedly UP/DOWN or runaway, so it will be undefined behavior.

Q	Please tell the voltage specification of S1˜S4 input signals.
A	Input signal voltage range of each terminals must be −0.3～VCC+0.3V (absolute maximum rating specification) to prevent IC damage. Normally it works around VCC/2. For the signal level adjustment of operational setting, instead of adjusting terminal S1˜S4, please adjust SINMNT/COSMNT voltage level which is 2～3Vp-p with V_{COM} potential center.

Q	As a noise countermeasure, would like to add normal-mode-capacitor C_N . How much capacitor value do you recommend?
A	C_N insertion is required as counter action for some negative effect of electorical noise injection. Actual cap value can not specify due to it depend on the noise level. Too large cap value might cause larger attenuation and phase change of resolver signals. So C_N value variability might cause an imbarance between SIN and COS, and it becomes error factor. Be careful about it.

Q	In case of monitor output exceed 3.8Vp-p, what kind of adverse effects can we expect?
A	It is assumed like voltage saturation and abnormal waveform for monitor output. These will be error factors for R/D conversion.

Q	Specification said that the phase difference between R1−R2 voltage phase and exciting component phase of resolver monitor signal(COSMNT,SINMNT) should be within±45° when R1/R2 terminals use as external exciting signal input mode. If phase difference is over ±45° , what kind of actual impact can we face?
A	When phase difference shows over 45° , it takes time to settle angular output at startup, or in worst case it can not settle forever. Also when there is a steep angle change of resolver, IC might not be able to respond or takes long time to catch up. When R1/R2 terminals use as external exciting signal input mode, the input signal phase between R1−R2 is used for synchronous detection with automatic phase correction. If the phase difference shows over the acceptable value, it cause a phase shift of the synchronous detection. Equivarently negative feedback control loop gain that realize R/D conversion is getting decrease and dynamic transfer characteristic have some impact, so such symptoms appears.

Q	Though we want to use the R1/R2 terminals as external excitation signal input mode , the phase difference between R1−R2 voltage phase and exciting component phase of resolver monitor signal(COSMNT,SINMNT) shows over 45° . How can we treat it in such case?
A	When phase difference shows over ±45° , please make the phase adjustment in the input circuit of external resolver excitation signal. It will enable the normal R/D conversion if you adjust the phase shift value (within ±45°) between R1−R2 voltage phase and exciting component phase of resolver monitor signal(COSMNT,SINMNT).

■Questions about the default setting function.

Q	Trying to set the default setting terminals for pull-up side. The default setting terminals have internal pull-up resistor. Still do we need to add external 10kΩ pull-up resistor for setting pull-up side?
A	In functiobnal view point, the terminal will be pull-up setting without external 10kΩ pull-up resistor. But internal pull-up resistor value of IC is large one so in terms of noise immunity it is weak. Then we recommend to add external 10kΩ pull-up resistor.

Q	There is an excitation mode selection in default setting function. What is difference between current excitation mode and voltage excitation mode?
A	An excitation mode setting function sets the allowable range of the internal phase shift according to the phase shift value caused by the situation of the peripheral circuits when you use exciting output function of AU6805. This IC's acceptable range of the phase shift between an excitation waveform component of R1-R2 current output and an excitation waveform component of the output voltage monitor is as follows. ■Current excitation mode : +90° ±45° ■Voltage excitation mode : 0° ±45° A main impedance of resolver will be L component and depending on excitaion type there will be different phase value between an excitation waveform component of R1-R2 current output (source of excitation signal) and an excitation voltage phase. That is why we provided this function. Since this is a function to change the internal setting, excitation output between R1-R2 is not changed by this setting difference.

Q	Are there any effects when we used a situation which exceeds the allowable range for each phase shift in the excitation mode setting?
A	It is possible to happen the cases which takes long time to angle settling at startup, or which do not settle even forever in the worst case. Also it is possible the cases which can not respond when a steep angle change has occurred in the resolver, or take long time to response.

■Questions about the serial input setting function.

Q	While setting the serial, what happen in the situations which send less than 12 bits data and SSCS set to “H” ?
A	Less than 12 Bits data of serial input is invalid. So serial setting register can not update.

Q	While setting the serial, what happen in the situations which send longer than 12 bits data and SSCS set to “H” ?
A	This is a shift register so last 12 input data was set in 12 shift register. Other data before last 12bit data is discarded. Let’s assume that when you enter up to 16 Bits. The contents of 5Bit ~ 16Bit input data can be set in serial setting 12 bit register.

■Questions about the output interface.

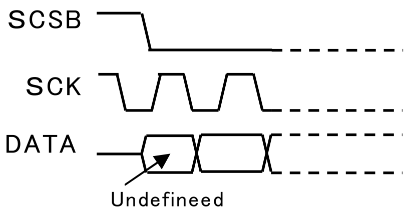
Q	In the situation of digital output terminals might be shorted each other , short to VDD or GND, what kind of issues will be appear when the power is active?
A	When the voltage is different between the shorted pin (One side “H” and the other side “L”), excessive current flow from “H” to “L”, heating up, and finally IC might be damaged.

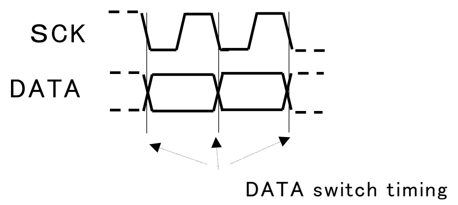
Q	Would like to get 8bit parallel output data. How can I do?
A	If you ignore the lower 4 bits, remaining data looks like 8 bits.

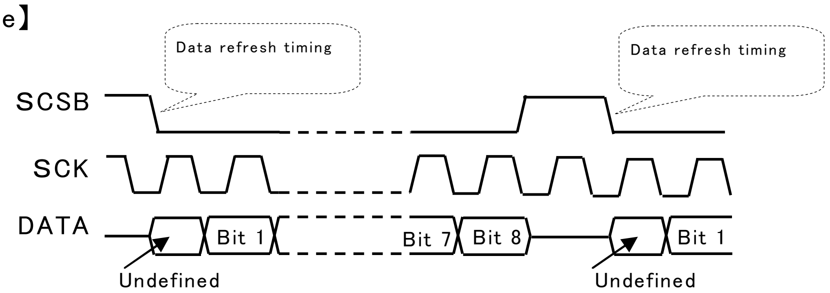
Q	Is A/B/Z output from the parallel data pin (Pulse equivalent to encorder mode) the same as A/B/Z output of independent terminal? Is it possible to be used at the same time also?
A	It is the same output. And it is also possible to use at same time.

Q	Using encorder equivalent pulse mode, A/B pulse duty looks unstable while resolver rotate with same speed. What is possible cause?
A	Encorder equivalent pulse output of this IC is theoretically poorer performance than optical encorder pulse output. Due to the affect of resolver potential error and R/D potential error and also R/D conversion principle itself, it is possible to be disordered pulse duty even if in normal operation condition.

Q	For the digital output, serial interface output and parallel interface output and also independent terminal A/B/Z output are prepared. Do we need to use all output?
A	On the behavior of this product it is not a problem even if it uses the output of either. According to the system environment, please use appropriate interface or output.

Q	In serial output case, after SCSB falling edge, is the data which is before first SCK falling edge unnecessary?
A	No need. After SCSB falling edge, output data which shows until SCK falling edge is undefined value. Please ignore it. 

Q	To read the serial output data with above system, which is better trigger? SCK rising edge or SCK falling edge?
A	Please use SCK rising edge. Serial output data change with SCK falling edge timing. Then if you read the data with SCK falling edge, there might read false data depending on read timing. 

Q	Plan to use serial output function with absolute output mode. But data need only 8bit due to above system configuration. How should I handle about serial output data?
A	Please exit serial output sequence （SCSB=L⇒H） after 8th serial data output. ※Even in the middle to end, data is refreshed and next output mode start with MSB data. 【Example】 

Q	Serial output mode(SCSB=L) keep with more than 16 SCK clock. What kind of behavior happen?
A	When you input SCK continuously with SCAB=L condition, serial output data will be repeated each 16 SCK clock period.

■Questions about the external clock.

Q	When this product operates in external clock mode, is it possible to connect crystal oscillator or ceramic resonator directly as external clock input?
A	Can not be connected. It must be only digital clock signal generated by crystal oscillator, etc.

Q	In external clock mode, clock frequency specification shows 10MHz±30%. When a clock which exceed its frequency range applied, what kind of problem does it happen?
A	It might be considered as malfunction of abnormal detection function.

■Questions about the power sources.

Q	What kind of problem does it expect if you do not used in the same potential VCC, VRR, and VDD？
A	It may cause abnormal heat generation or failure. Each power supply is connected through a diode. When the potential applied to diode is getting bigger than the diode forward voltage, excessive current will generate.

Q	When the power is turned on, what problem are you having not been turned on at the same time VCC, VRR, and VDD.
A	There is possibility not to make default setting correctly. The power-on reset has been granted to the VCC pin. While pull-up/pull-down of default setting terminal usually connect to VDD potential. If VCC is applied but VDD is not applied, in this case there might be miss-setting in default setting sequence and incorrect data might be read. Also each power supply is connected through a diode. When the potential applied to diode is getting bigger than the diode forward voltage, excessive current will generate and it might cause potential problem.

Q	I would like to excite resolver with external voltage booster amplifier which signal source is exciting output of AU6805. Is there any timing constraint for the exciting amplifier power up?
A	There is no special restriction. If the power supply of exciting amplifier turns on after the device power supply, the device will not be able to get resolver input signal. Then it might cause fault detection with the balance of the mask error period.

■Questions about the function of fault detection.

Q	Does the fault detection result affect the behavior of R/D conversion?
A	Does not affect. The fault detection function is independent to R/D conversion so fault detection result does not give a constraint on the output of R/D conversion. It will continue to operate R/D conversion as abnormal condition. But when it return to the normal state from abnormal resolver signal state or breaking of resolver signal line, it try to shorten the R/D return operation period by using auto-tuning mode of loop gain as tempolary.

Q	When the error reset at ERRSTB, How long time do we need to set reset situation (ERRSTB=L) ?
A	Minimum 220ns (Same as maximum time to be extended ERRHLD signal)

Q	Does the error reset function by ERRSTB affect the behavior of R/D conversion?
A	Does not affect. ERRSTB is a function to reset ERRHLD and ERRCD1～3 outputs only.

Q	DC bias resistance was connected in reverse polarity. Nevertheless error detection looks work at signal desiconnection situation. Why is the error detected?
A	Depending on the angle there might be detected failure by abnormal resolver signal. And due to connect in reverse polarity, in disconnection case, monitor output voltage expect shift to GND-side. Then correct R/D conversion can not operate and it is considered that abnormality have been detected by abnormal R/D conversion.

Q	During 35ms (max.) error mask period after VCC up, what is ERR/ERRHLD output behavior?。
A	L output will be forced regardless of abnormality detection in this product.

■Questions about the function of Built-In Self-Test(BIST) and Special mode

Q	If want to run consecutively to excute self-test (BIST), Does error resetting activity need to run in every BIST operation?
A	Error reset can be performed only once after running the last self-test(BIST) operation. ERRHLD "H" output during the excution of the BIST will be remained even if it returns to normal operation after BIST. Then error reset operation is required.

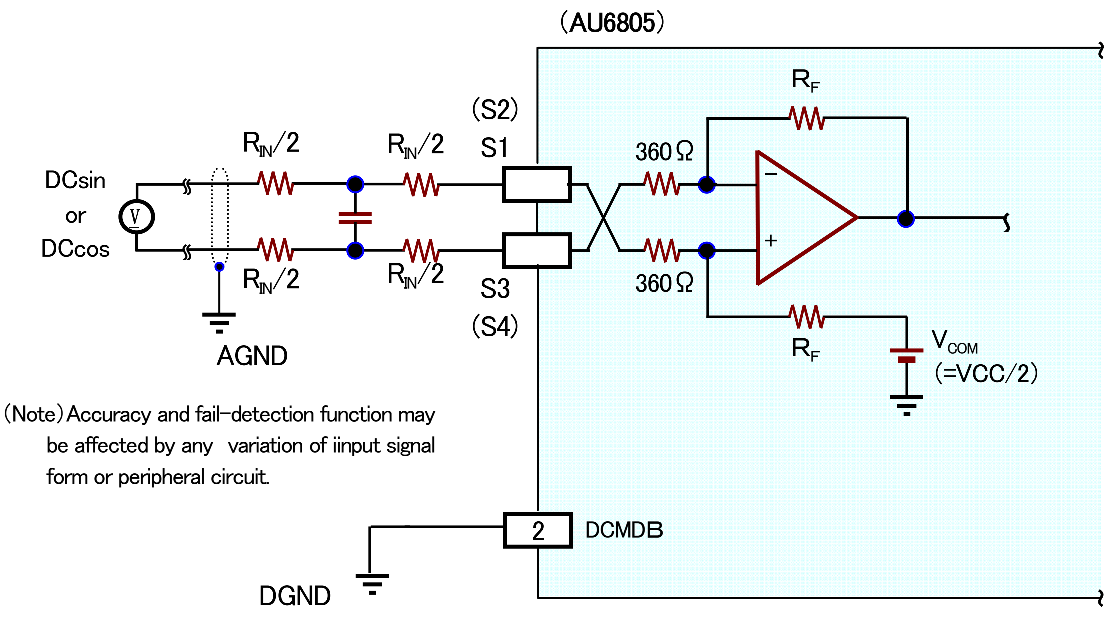
Q	Operating BIST operation or special mode, please tell the conditions when BIST result show "abnormal BIST (BIST code "1111")".
A	There are two cases explained below. ■The case that the BIST result is NG at the time of serial output. ■The case that you run BIST sequence with "a reserved BIST setting code" or "a special mode" of serial input setting register.

■Questions about the applications.

Q	Is it possible to use with phase modulation type (BRT) resolver?
A	No. This product only supports amplitude modulation type (BRX) resolver.

Q	Is it possible to use multiple AU6805 which connect same one resolver?
A	Possible. Please set one AU6805 device with EXMDB="H" (excitation current output mode) , R/D conversion of resolver signal can operate with exciting the resolver using the excitation current output. The other AU6805 devices set as EXMDB="L" (External excitation signal input mode), then multiple usage is possible by entering the resolver excitation signal to R1/R2 terminal.

Q	How much cable length between resolver and AU6805 can we extend?
A	It can not to say simple because it depend on the type of cable and wiring, but basically there are not much problem about cable length itself which is a few meters except for noise superimposed, etc.

Q	Please explain the sensor selection function (setting DCMDB terminal).
A	This function assumed the R/D conversion with the DC resolver signal. Though originally resolver signal (k・sinθ・sinωt, k・cosθ・sinωt) contains exciting components (sinωt), this IC is able to function effectively even if DC resolver signal (E・sinθ, E・cosθ) without exciting components. Set DCMDB="L" and input DC esolver signal to resolver signal input circuit. 

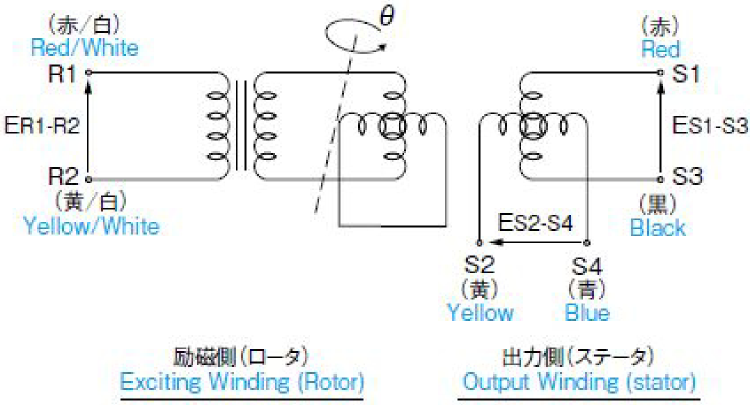
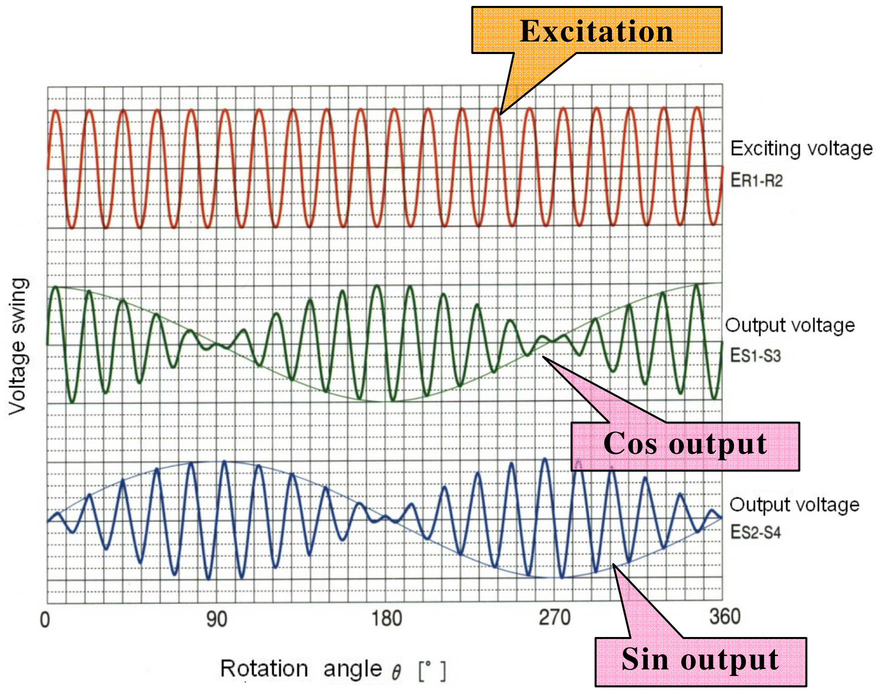
11.4 Terms and Definitions

Term	Number of multiple(N)
Definition	Show 1/2 the number of poles(pole pair). Display is added with ”X”.

Term	Mechanical angle(θ m)
Definition	Rotational angle of resolver rotor(Mechine axis)

Term	Electorical angle(θ e)
Definition	Machine 1 cycle 360° /N(number of multiple) define as electorical 1 cycle 360° . θ e=N θ m

Term	Resolver input impedance(Zro)
Definition	Resolver exciting-side impedance

Term	BRX
Definition	1Phases-in/2Phases-out(Amplitude moduration type)brushless resolver. ■Configuration of resolver  ■Output voltage equation Excitation : $E_{R1\text{-}R2} = E_1 \sin \omega t$ Output : $E_{S1\text{-}S3} = kE_1 \cos\theta \sin \omega t$ $E_{S2\text{-}S4} = kE_1 \sin\theta \sin \omega t$ ■Exciting signal and resolver signal waveform 

12. Revision history

Revised date	Revision	Location of revisions	Revision content・reason
2016.3.30	First edition	—	Reference document is MNL000542W00 (Manual –Japanese version 2nd edition).
2016.4.6	Second edition	—	Revised the documentation layout.